SIGMA DESIGNS®

EM8550/EM8551 Datasheet

Single chip digital media processor for SDTV consumer appliances

Documentation for EM8550/EM8551

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Preliminary Information: Contains information on a product under development. Features, functionality, and parametric information are target goals, and are subject to change.

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Tel: 408.262.9003 • Fax: 408.262.9740 • www.sigmadesigns.com • sales@sigmadesigns.com

EM8550/EM8551 Datasheet

Single chip digital media processor for SDTV consumer appliances

Features

Host block

- 32-bit RISC processor
- 16 KB cache
- 8 KB SRAM on-chip
- Interrupt controller
- Two timers, including a watchdog timer

SDRAM and flash ROM memory

- Up to 16 MB system memory
- Up to 4 MB flash-memory support

IO standards

- Standard IDE (ATA/ATAPI-4/UltraDMA)
- Sony and Sanyo DVD loader system
- Synchronous 8-bit parallel interface (SPI) up to 20 Mbps
- I^2S interface (master or slave mode) up to 20 Mbps
- Two serial interface UART
- I^2C master or slave mode
- Local bus interface supporting Ethernet chipsets and MPEG encoders
- 32-bit general purpose I/O

Audio interface

- I^2S output
- Digital serial S/PDIF output

Video interface

- NTSC/PAL TV encoder with 4 video DACs
- Macrovision 7.0.1 copy protection support for EM8550 only; EM8551 does not support Macrovision
- Analog composite, S-Video output, component YPrPb & RGB
- Four 10-bit video DACs supporting up to 80 MHz pixel clock
- 480p YPrPb output
- Digital component 8/16-bit YUV (CCIR 601, CCIR 656, NTSC, PAL) and 24-bit RGB
- Progressive or interlaced analog/digital video ouputs
- Built-in high quality scaler to support any VGA or HDTV output resolution (analog and digital)
- Multiple output frame rates from 50 to 100 Hz

DVD support

- CSS Decryption, 16:9, 4:3 playback and letterbox, 3:2 pull down
- Full DVD navigation, multiple angles, sub-picture, 8-bit 256-color OSD with scaler
- DVD sub-picture

Video decoding

- MPEG-1 and MPEG-2 decoding
- MPEG-4 advance simple profile without GMC and QPEL
- JPEG still images

Video input

- Digital input: 16 bit YUV 4:2:2 (CCIR 601/656)
- Master/slave modes

Audio decoding

- MPEG-2, MPEG-1 layer 2, MP3, low complexity AAC, AC-3, WMA
- Audio sampling rates of 32, 44.1, 48,88.2, 96kHz

Media formats

- DVD-Video, Superbit DVD, Kodak picture CD, SVCD, VCD 1.x, VCD 2.x, CD-DA, CD-ROM

Front end interface

- IDE, DVD loader, VFD interface

On screen display

- 2-, 4-, 7-, and 8-bit per pixel from 24-bit palette
  - Programmable OSD scaler
  - Programmable flicker filter for interfaced output modes
  - Alpha blending over video (16 levels)

Software support

- Integrated real time operating system: μC Linux
- DVD navigation

Package

- 501 BGA
- 0.18 micron CMOS technology

Power

- 3.3V and 1.8V operating voltages
- Low power (1.2W) max and power down modes

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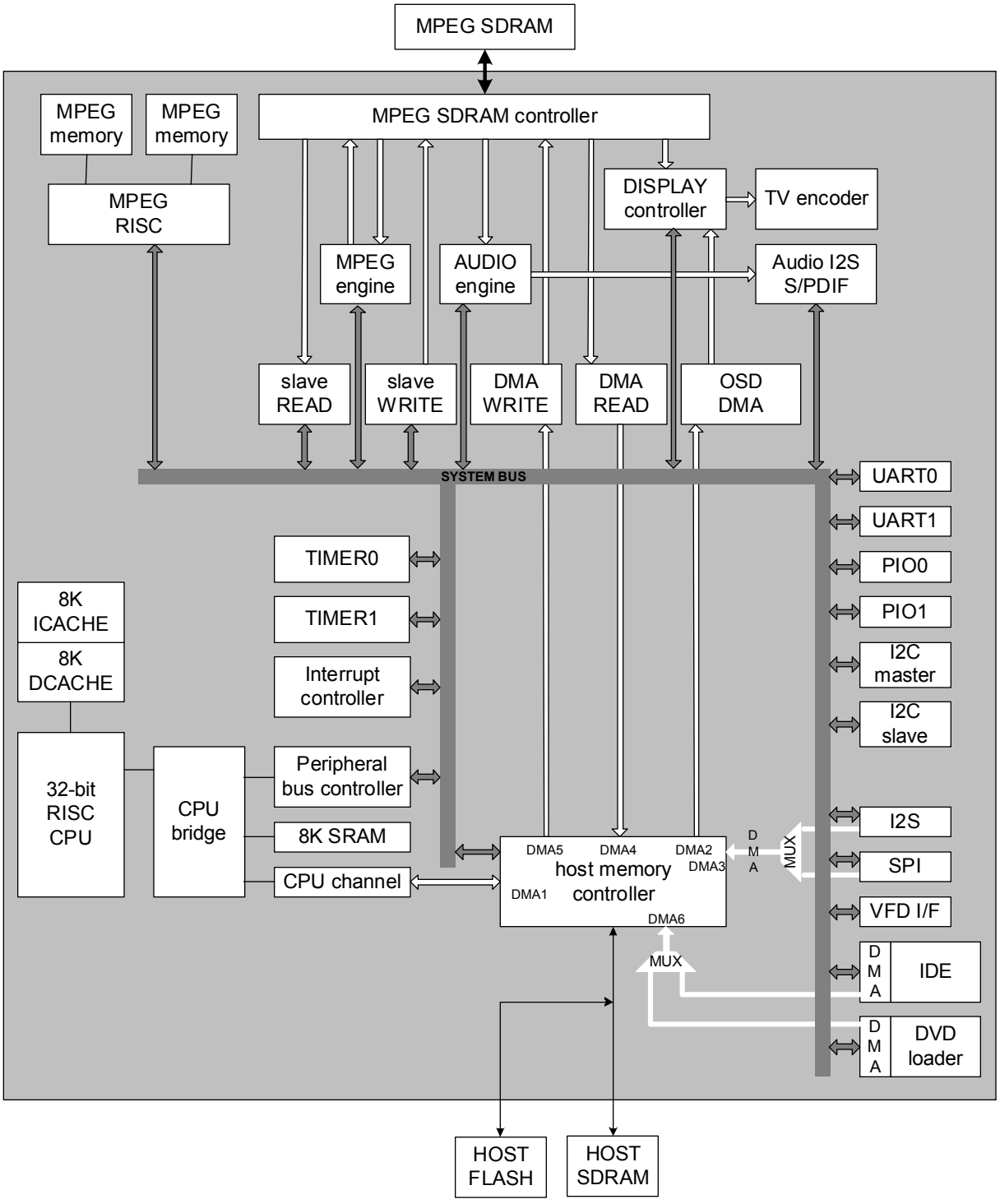

Figure 1. EM8550 block diagram.

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Overview

The EM8550 is a single chip solution that facilitates the design of a large variety of cost-effective, feature-rich SDRV consumer appliances. This highly integrated solution supports a multitude of audio/video decoding standards such as VCD, DVD-Video, AC-3, AAC, and MP3. In addition to supporting popular entertainment standards, the EM8550 supports AVI, ISO MPEG-4, DivX formats and still JPEG images.

System and processor control

System and processor control functions include interfacing the CPU to the rest of the chip and monitoring CPU requests for illegal accesses. The system and processor control blocks include the Peripheral Bus Controller, the CPU MBus Channel, and the System Configuration registers.

Clock control

The system clock is derived from an external clock pin. The clock is buffered and distributed throughout the chip. The system control block also controls and distributes the reset condition to all blocks.

Interrupt controller

The interrupt controller allows each interrupt to be asserted as either of two interrupt levels, FIQ or IRQ. This allows interrupt to be used for application-specific needs, while still fulfilling real-time requirements. Each interrupt may be individually masked; alternatively, all interrupts may be masked without altering the individual interrupt masks.

Memory access controller

The Memory Access Controller (MAC) provides access to external memory. It arbitrates access between the CPU, and six independent DMA channels.

The MAC provides control and access for 16 or 32 bits of ROM or Flash for boot-up. One port is provided for 32 bits of SDRAM. The EM8550 supports up to 16MB of SDRAM using a 32-bit interface.

Timer

The timer block contains two independent timers, each with several modes of operation. A mode register allows selection between a free-running timer, a periodic interrupt, or a timeout function which generates a single interrupt. The second timer includes a watchdog mode, which resets the processor when a timeout occurs. A prescaler allows greater time periods when resolution is not critical.

Peripheral interface

Universal Asynchronous Receiver-Transmitter

The UART550-compatible Universal Asynchronous Receiver-Transmitter block provides serial communication and debugging with full modem support that allows simultaneous connection to remote systems.

IDE interface and DVD loader

The IDE controller and DVD loader interface comprise the front end interface and share the same pins. The IDE controller supports PIO, DMA, and UDMA-33 modes. The standard 16-bit IDE interface supports up to mode 4.

The DVD loader interface module communicates with the external DVD loader through an 8-bit AV interface and a serial host interface channel. DVD loaders supported include those from Sony and Sanyo. The DVD-DMA controller provides a DMA transfer from the DVD loader to external (SDRAM) memory. The processor may perform other tasks while large blocks of data are transferred to memory.

I^2C master and slave

This I^2C master controller, which supports the synchronous Inter Integrated Circuits (I^2C) serial protocol, enables the Host CPU to access an external I^2C slave device using a simplified register interface, or act as an I^2C slave device. It accommodates bi-directional data transfer, has a programmable address width of up to eight bits with sequential byte read or write capability, and generates interrupts whenever bytes are transmitted or received.

I^2S block

The I^2S block receives data from a I^2S compliant transmitter and supports both master and slave modes with a maximum data rate of 20 Mbps. In both modes the data is always accepted as MSB first/high bytes first.

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SPI block

The SPI block accepts data from an external device through an SPI interface. When the SPI/I^2S block is in DMA transfer mode, the SI bus can transfer data at rates of up to 20 Mbit/s.

Local bus interface

The local bus interface is a 16-bit multiplexed address data bus. In incorporates a DMA engine for transferring data from external devices to memory. It supports numerous devices, including the Cirrus Logic CS92288 MPEG-2 encoder.

General purpose I/O controller

The general purpose I/O controller provides 32 pins of general purpose control signals and logic to help eliminate the glue logic necessary for system integration. Its functions include indicating system operation or controlling other devices.

Audio

The audio decoder supports CDDA, DVD-audio with MLP option, Kodak Picture CD, Dolby® Digital 5.1 channel, MPEG-1 layers 1, 2 and 3 (MP3), MPEG-2, AAC, and Copy Protection for Prerecorded Media (CPPM). A 6-channel external DAC will support full 5.1 high-quality audio.

Audio ouput

The EM8550 sends digital audio to the S/PDIF output for high quality audio performance. The 5.1 channel audio can be downmixed for two channel output.

Video

Video processing

The EM8550 decodes MPEG-1, MPEG-2 and MPEG-4 video. The decoder handles MPEG-2 and MPEG-4 streams up to 720x480p or 720x576i source at MP@ML. JPEG decoding outputs up to 1920x1080 true resolution in 1080i mode.

Video output

The EM8550 support Composite, S-video, and Component outputs for high quality video playback. The chip also has a 24-bit RGB output that connects gluelessly to a Digitial Video Interface (DVI) device with High Definition Content Protection (HDCP).

On Screen Display

The EM8550 has an integrated On-Screen Display (OSD) unit. This can be used to overlay graphics content such as a DVD user interface or graphics images over the video window with 16 levels of alpha blending. The OSD includes a scaler to support all output resolutions, as well as 16 levels of flicker filter for interlaces output modes.

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The figure below illustrates a DVD player incorporating the EM8550. The highly integrated silicon connects directly to DVD system peripherals without glue logic.

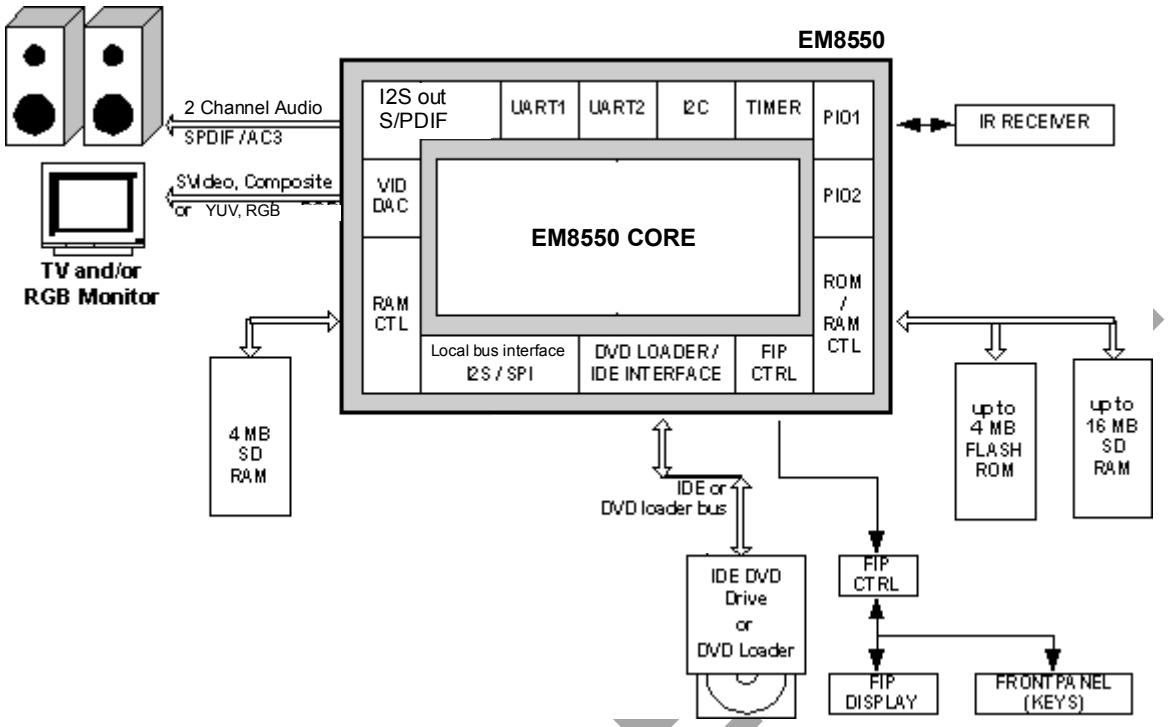

Figure 2. DVD block diagram.

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System and Processor Control

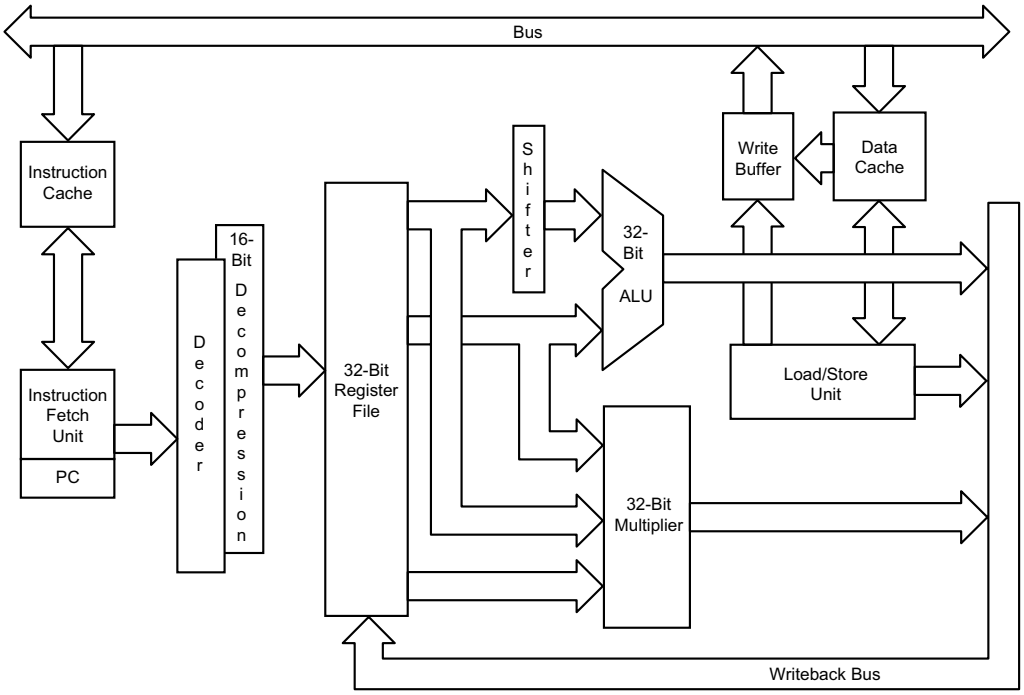

Figure 3. System and processor control block diagram.

The EM8550 integrates a powerful 32-bit RISC processor optimized for multimedia acceleration. The RISC handles all system activities, including, for example, navigation, demux, and system management.

General functions

The chip name, number and version number are available in read-only registers. The chip can be reset using software and power consumption can be adjusted by varying the PLL speed.

Internal memory

The internal memory is comprised of 8K of SRAM which is both read and write byte-accessible. All accesses are zero wait states. A remap function allows internal SRAM to be remapped to the first 8KB of address space for processing FIQs and IRQs quickly.

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Interrupt Controller

The interrupt controller enables and disables each interrupt individually or globally. A 2-level interrupt priority selection can be implemented.

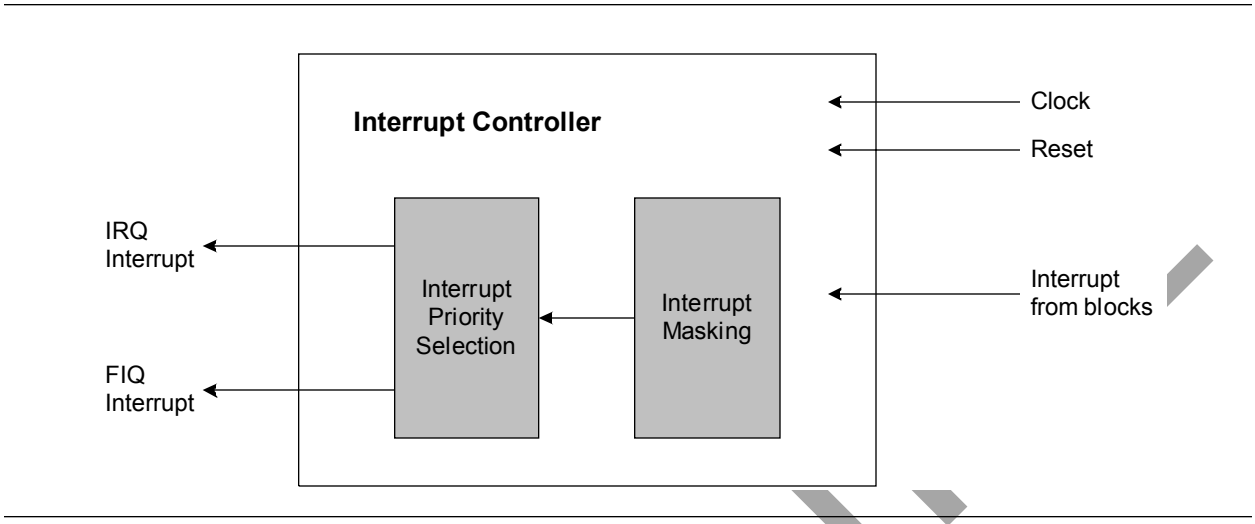

Figure 4. Interrupt controller block diagram.

Interrupt control

Each interrupt may be enabled or disabled, or a global disable may be enforced. Interrupts must be cleared at the source once the service request is served. All blocks with cascaded interrupt control provide an interrupt mask for each interrupt source and clear each source individually.

Interrupt sources include the following:

- Timer 1 and 0
- UART 1 and 0
- PIO 1 and 0
- I^2C master
- DVD loader
- IDE interface
- I^2S interface
- SPI interface
- MPEG core

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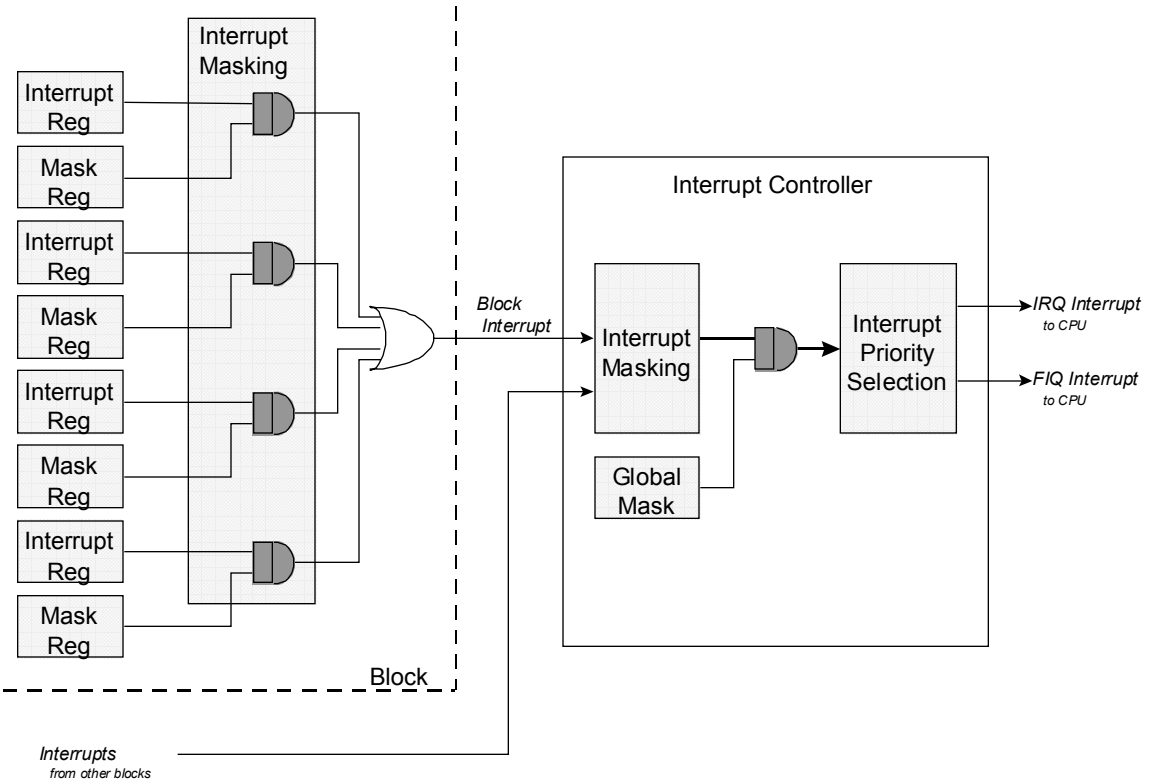

Figure 5. Cascaded interrupt structure.

Interrupt priority

Each interrupt may be assigned a priority of IRQ or FIQ, allowing software to customize the priority of each block. See "Application Notes" for more information on multi-level interrupt control.

Global disable

The Interrupt Controller provides a global disable control bit. Use this feature to avoid interrupting a critical portion of code before completion. Global disable does not affect the individual interrupt masks. Software need not perform a save and restore. This saves time by reducing code size and interrupt latency if an interrupt is asserted while all interrupts are disabled.

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Memory Access Controller (MAC)

The Memory Access Controller (MAC) is used to control external memory devices such as Flash, ROM/PROM and SDRAM.

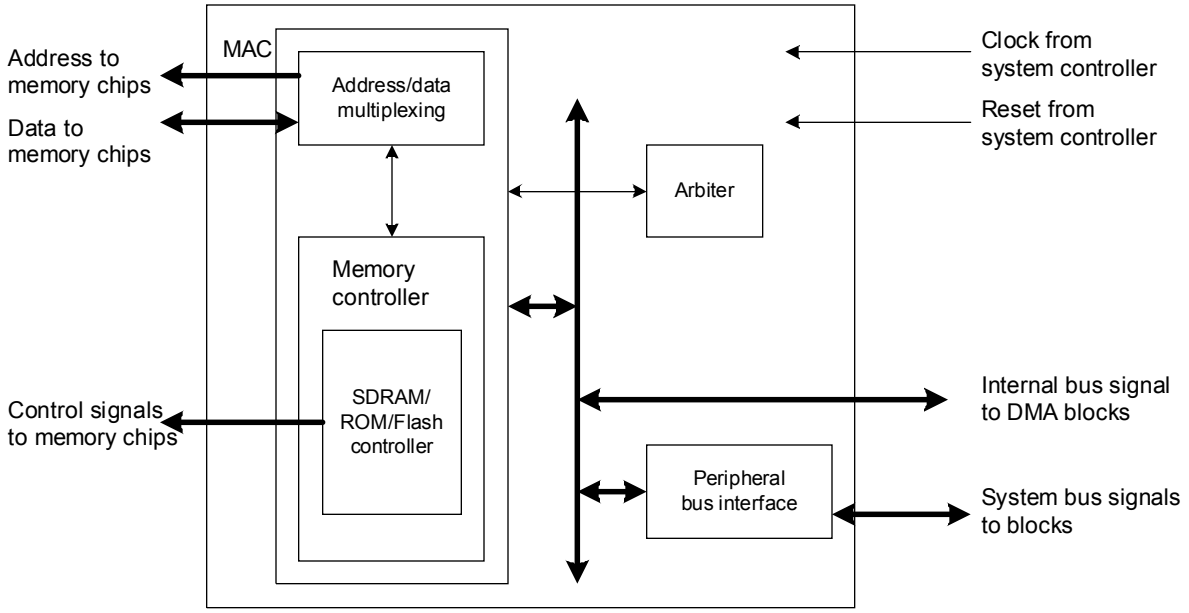

Figure 6. EM8550 memory address controller diagram.

Memory configurations

The EM8550 supports the following memory types: SDRAM, Flash, ROM, OTP, and EEPROM, among others. It also provides two types of interfaces: Flash and SDRAM. Up to 4MB of flash memory is supported using either a 16- or 32-bit interface. Up to 16MB of SDRAM memory is supported using a 16- or 32- bit interface.

Memory configuration selection

Memory width selection is accomplished through external configuration pins. At power-up, memory speeds are set to the slowest supported setting to allow maximum compatibility. Firmware may change the speed settings during boot-up.

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The diagram below details the memory map of the EM8550. It provides an overview of where each block of device/address information resides.

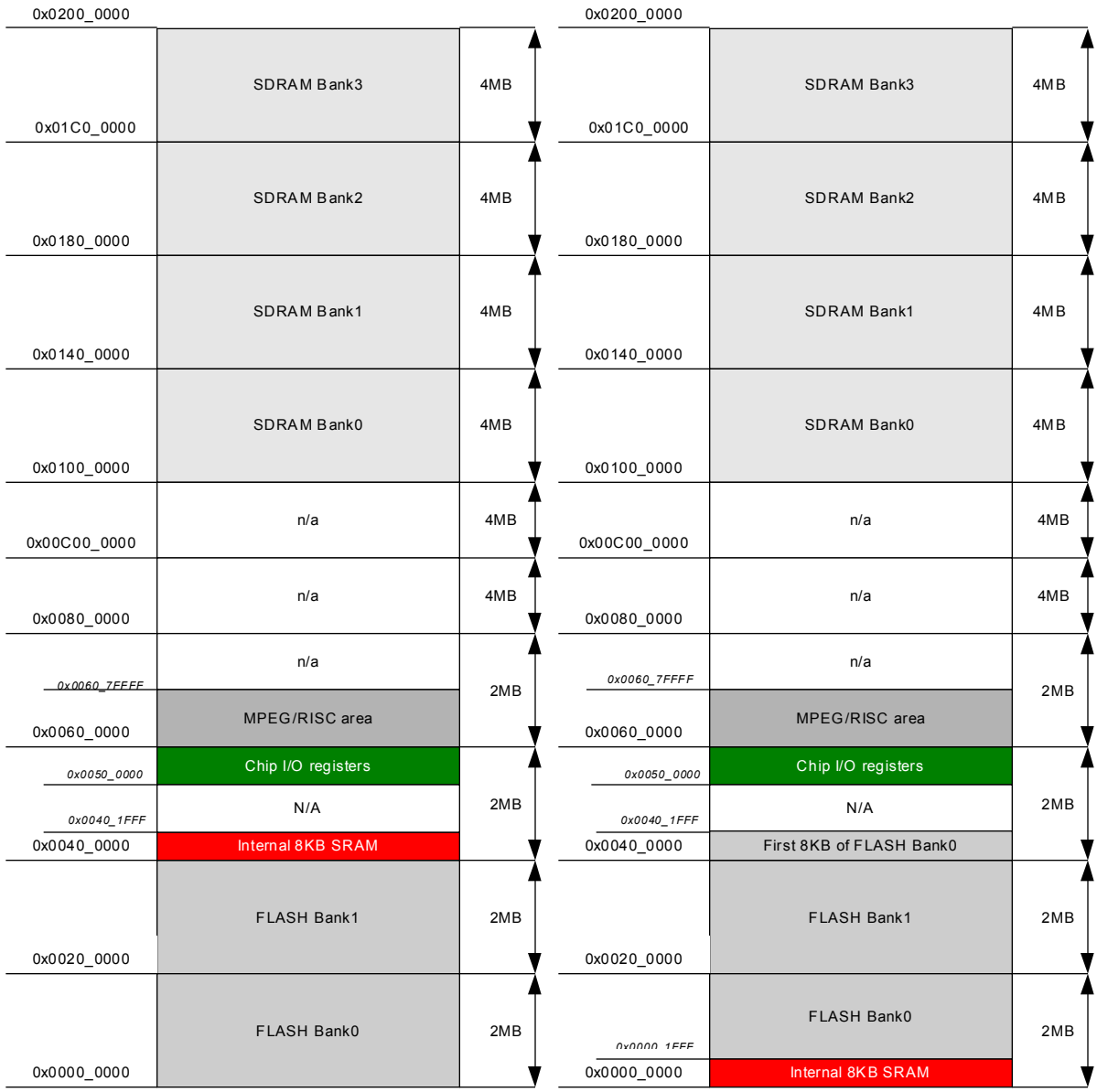

Figure 7. EM8550 memory map.

DMA channels

Direct Memory Access transfers data from one system peripheral to another with minimal CPU intervention. To intiate the process, program the starting address, destination address, and the byte count to transfer. The EM8500 supports six DMA channel for optimal performance.

- DMA1 = CPU channel

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- DMA2 = OSD channel
- DMA3 = I^2S/SPI channel
- DMA4 = Master Write channel
- DMA5 = Master Read channel
- DMA6 = IDE/DVD channel

Flash memory

Flash memory typically contains firmware code, system level software, boot loader and operating system. The EM8550 supports up to 4MB of flash memory. The memory configuration is set using FLASHCFG[1:0] configuration inputs.

Table 1. Flash memory configurations.

FLASH	Total mem.	Memory configuration	Uses			Board Configuration (IC Config) x #ICs	FLASHCFG [1..0]
			ICs	CS#	A-Lines		
1	2 MB	1 M x 16 bit	1	1	A[19..0]	(1 M x 16 bit) x 1 IC	0 0
2	4 MB	2 M x 16 bit	1	1	A[20..0]	(2 M x 16 bit) x 1 IC	0 0
3	4 MB	1 M x 32 bit	2	1	A[19..0]	(1 M x 16 bit) x 2 ICs	0 1
4	4 MB	2 M x 16 bit	2	2	A[19..0]	(1 M x 16 bit) x 2 ICs	1 0

Powerup strapping on FLASHCFG [1..0] is required to determine flash configuration.

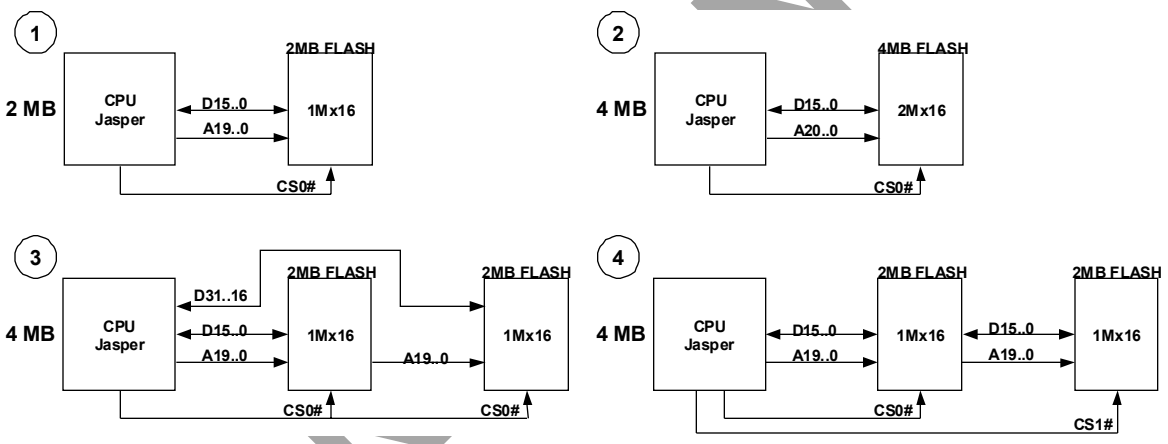

Figure 8. Flash memory configuration diagrams.

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SDRAM memory

SDRAM typically contains applications, firmware, and an operating system to execute local code. The EM8550 supports up to 16MB of SD-RAM/SG-RAM memory. Firmware sets memory configurations.

Table 2. SDRAM memory configurations.

RAM	Total mem.(1)	Memory config	Uses						Board configuration (IC Config) x #ICs
			IC	Bank	CS#	Addr.	RAS#	CAS#	
1	2 MB SG	512K x 32 bit	1	2	1	A[9..0]	A[9..0]	A[7..0]	(512K x 32 bit) x 1
2	4 MB SG	1 M x 32 bit	1	2	1	A[10..0]	A[10..0]	A[7..0]	(1M x 32 bit) x 1
3	4 MB SD	1 M x 32 bit	2	2	1	A[10..0]	A[10..0]	A[7..0]	(1M x 16 bit) x 2
4	8 MB SD	2 M x 32 bit	1	4	1	A[10..0]	A[10..0]	A[7..0]	(2M x 32 bit) x 1
5	16 MB SD	4 M x 32 bit	1	4	1	A[11..0]	A[11..0]	A[7..0]	(4M x 32 bit) x 1
6	16 MB SD	4 M x 32 bit	2	4	1	A[11..0]	A[11..0]	A[7..0]	(4M x 16 bit) x 2

1. Typical DVD playback requires at least 8 MB of system memory.

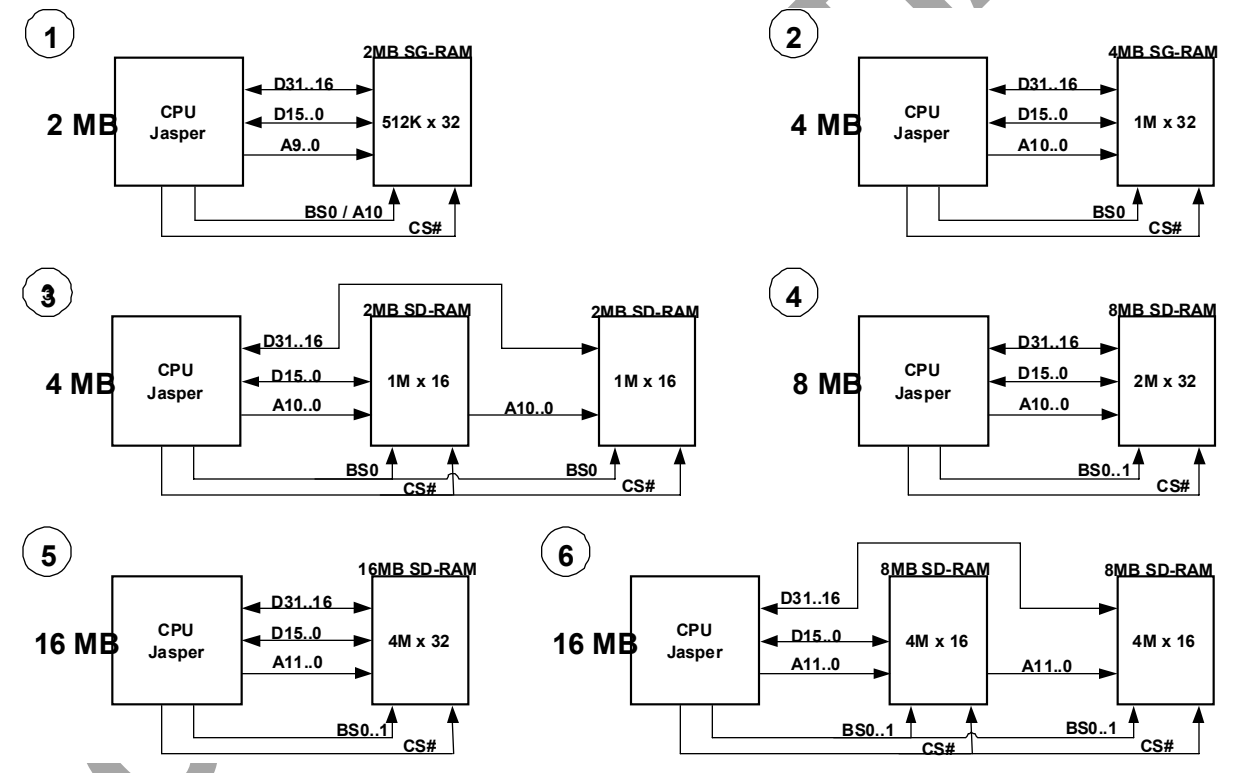

Figure 9. SDRAM memory configuration diagrams.

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Table 3. Memory bank select.

Quantity	Chip configuration
2MB	SGRAM 512K x 32
4MB	SGRAM 1M x 32
4MB	SDRAM 1M x 16 (x2)
8MB	SDRAM 2M x 32
16MB	SDRAM 4M x 32
16MB	SDRAM 4M x 16 (x2)

Memory Timing Control

To support multiple memory types and configurations, the EM8550 provides timing configuration control registers to adapt to selected memory types.

Flash timing

The following Flash timing parameters are programmable, and are illustrated below:

- Chip Select and Address setup
- Chip Select and Address hold
- Output Enable width
- Write Enable width

Table 4. Memory timing parameters with corresponding FLSHCFG and descriptions.

Parameter	FLSHCFG bits	Description
FLSHWADR	19:18	Address and Chip Select Setup to Write Enable
FLSHRADR	17:16	Address and Chip Select Setup to Output Enable
FLSHWE	15:12	Write Enable Assertion Time
FLSHOE	11:8	Output Enable Assertion Time
FLSHWHOLD	7:6	Data, Address and Chip Select Hold Time from Write Enable
FLSHRHOLD	5:4	Address and Chip Select Hold Time from Output Enable

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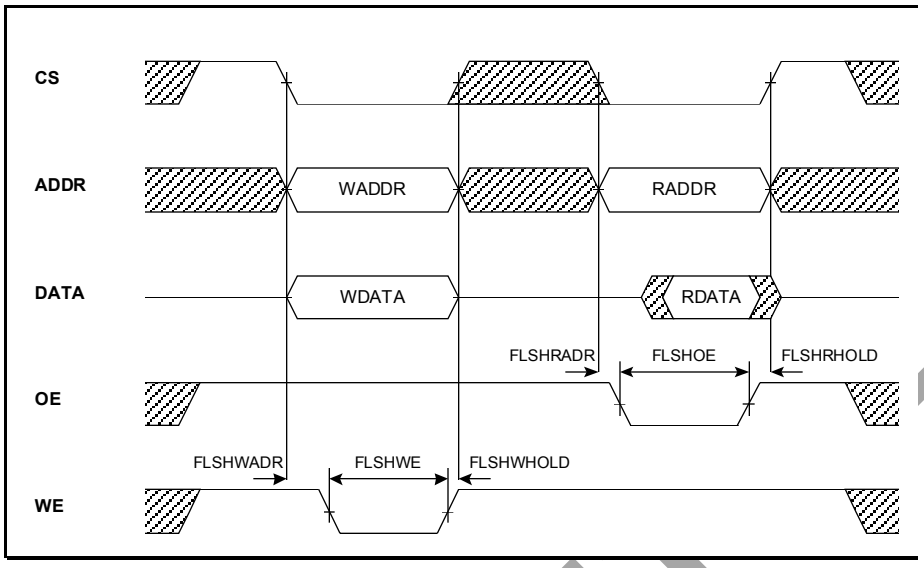

Figure 10. Programmable Flash timing parameters.

If FLSHRADR and FLSHRHOLD are both zero, Output Enable remains asserted for multiple consecutive accesses.

FLSHWADR and FLSHWHOLD cannot both be zero, or no rising edge of WE will be generated for strobing data into the memory device.

Neither FLSHWADR + FLSHWE + FLSHWHOLD nor FLSHRADR + FLSHOE + FLSHRHOLD may be less than three.

Arbiter

Many sub-blocks require access to system memory. There may be instances when multiple blocks require access during the same interval. To help direct traffic, the arbiter allocates access to the memory space based on the priority of the device. The arbiter allows devices to access memory in round-robin or modified round-robin fashion. The arbitration cycle is illustrated below, where the numbers indicate the priority when leaving a state.

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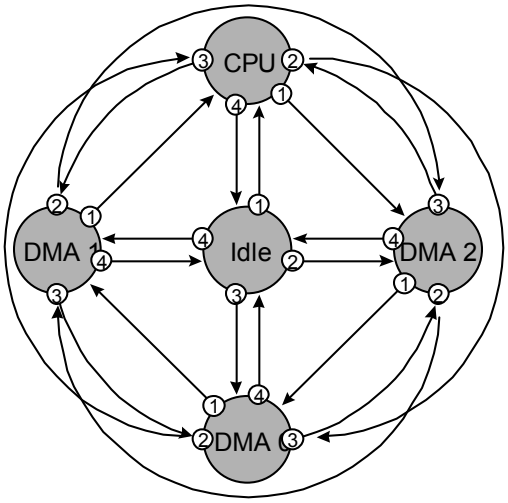

Figure 11. Arbitration cycle with four of six DMAs.

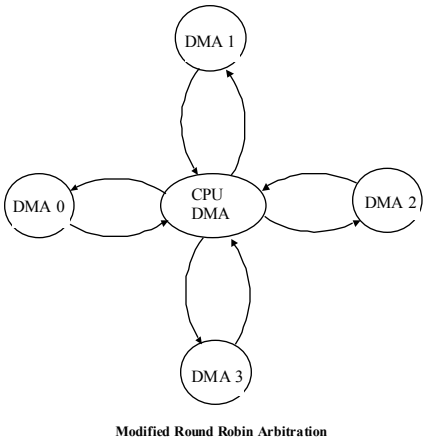

Figure 12. Modified round-robin arbitration.

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Timer

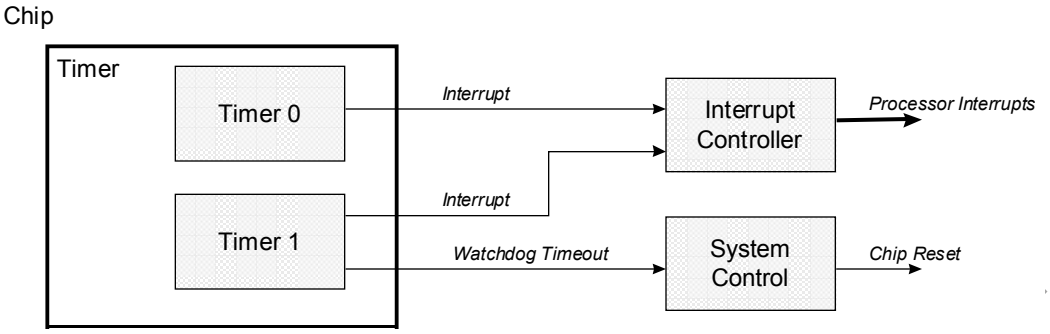

Figure 13. Timer block diagram (system overview).

The timer block includes two timers with scalable processor ticks. They count down from a user-loaded value, which must be reloaded to avoid a time-out. Each timer has an independent clock pre-scale function and an independent interrupt. They can be set to a periodic, free-running, or time-out mode. The second timer may be used as a watchdog timer, which resets the system on a time-out.

Timers are primarily used to accurately track long periods of time (such as during timeouts and internal performance monitoring), freeing the processor for more important tasks.

The timer is implemented as a 16-bit down counter. The timer counts down from the count value programmed in the timer **TMRxLOAD** register; on reaching zero, an interrupt is generated. Depending on the mode, the timer then reloads the load value, continues counting, or stops. The timer **TMRxLOAD** register can be changed at any time; the timer begins counting from the new value written to the **TMRxLOAD** register.

The timer powers up disabled. Write a '1' to the ***ENABLE*** bit to enable it, and disable it by writing a '0' to the ***ENABLE*** bit. When the timer is disabled, it stops counting and retains its current value. When it is re-enabled, it resumes counting from its current value. The timer can be reset at any time to the value in the **TMRxLOAD** register by writing the ***RESET*** bit in the **TMRxCTL** register with a '1.' The counter value immediately loads, whether or not the timer is enabled.

Clear timer interrupts through the **TMRSTAT** register. Read the interrupt bit to return the current interrupt status. Write a '1' to interrupt bits to clear the corresponding interrupts.

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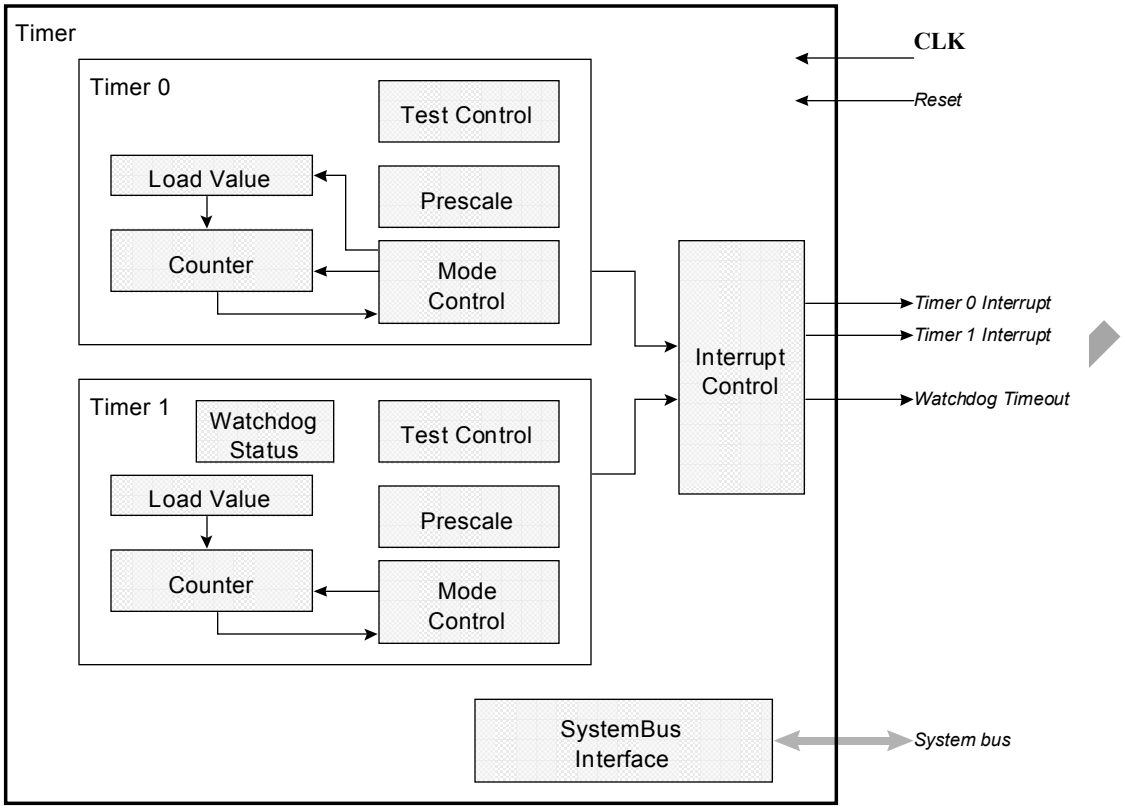

Figure 14. Timer block diagram (system overview).

Load value/counter

A counter, operating off of the system clock, drives the timer. The load value register, programmed by firmware, controls its period.

Prescale

A clock prescaler, provided to divide the timer counter clock frequency, allows larger time periods.

Mode control

Three modes of operation are available for Timer 0; four modes are available for Timer 1. Mode control controls the timer reloading and disabling.

Timer modes

Periodic

In periodic mode, the timer counts down to zero from the load value. An interrupt is generated when the count is zero. After reaching zero, the load value is reloaded into the timer and the timer counts down again. A load value of zero disables the timer.

Timeout

In timeout mode, the timer counts down to zero from the load value. An interrupt is generated when the count is zero. In this mode, the ***ENABLE*** bit is reset when the timer reaches zero, stopping the counter. After reaching zero, the load value is reloaded into the timer. A load value of zero disables the timer.

Free-running

In free-running mode, the timer counts down to zero from FFFFh. An interrupt is generated when the count is zero. After reaching zero, FFFFh is reloaded into the timer. The load register is ignored in this mode. This mode is identical to the periodic mode with a load value of 65535. Note that when the timer is first enabled, it begins counting down from its current value, not FFFFh.

Watchdog

In watchdog mode, the timer counts down to zero from the load value. If the load value is not reloaded or the timer is not disabled before the count is zero, the chip will be reset. When this occurs, every register in the chip is reset *except* the watchdog timeout status bit ***WDSTAT***; it remains set to alert firmware of the timeout event when it re-executes its bootstrap.

Watchdog mode is only available for Timer 1. The watchdog timeout status bit, ***WDSTAT***, is not reset when the watchdog timer resets the rest of the system; it is only reset by a power-on reset or when cleared by software. After a watchdog reset, software may check this bit during its bootstrap to determine if the system reset itself or whether it is booting up from a power-on reset condition.

Interrupt control

Each timer may generate an interrupt when it times out. In addition, Timer 1 can generate a watchdog timeout signal to reset the system.

System bus interface

The system bus interface block interfaces the timer registers to the processor through the system bus.

Clock pre-scale

A clock pre-scale is provided for the timer clock. Use the pre-scale to divide the system clock by powers of two, from 2^2 to 2^{16}.

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Universal Asynchronous Receiver/Transmitter (UART)

The Universal Asynchronous Receiver/Transmitter is a peripheral device for a computer. It converts internal data from parallel to serial format (or vice versa) for bidirectional transmission down a single cable. The device receives a character, generates an interrupt, and stores it in a buffer until the next character is ready. The CPU must fetch the information and clear the interrupt flag before the next character is sent to the buffer.

The UART uses a selectable internal or external clock that supports 5-8 data bits, 1-2 stop bits, even/odd/stick/no parity, and a 300-38400 baud rate. Its 16-byte transmit buffer interupts for empty data, and the 16-byte receiver interrupts for empty, half full, and byte-received data. The UART also detects false start bits, breaks and supports modem communications.

This UART550-compatible block provides an independent UART for serial communication and debugging. The UART includes full modem support, allowing simultaneous connections to remote systems. This UART is compatible with generic UART devices used on PCs and other systems. Proper start, parity, and stop bits are appended to characters transmitted on the TXD output pin. Similarly, the characters received at the RXD input pin are stripped of the extra bits enveloping them. Receiver and transmitter logic runs on the 16X clock derived from the main clock input divided by the value in the Clock Divider Control register.

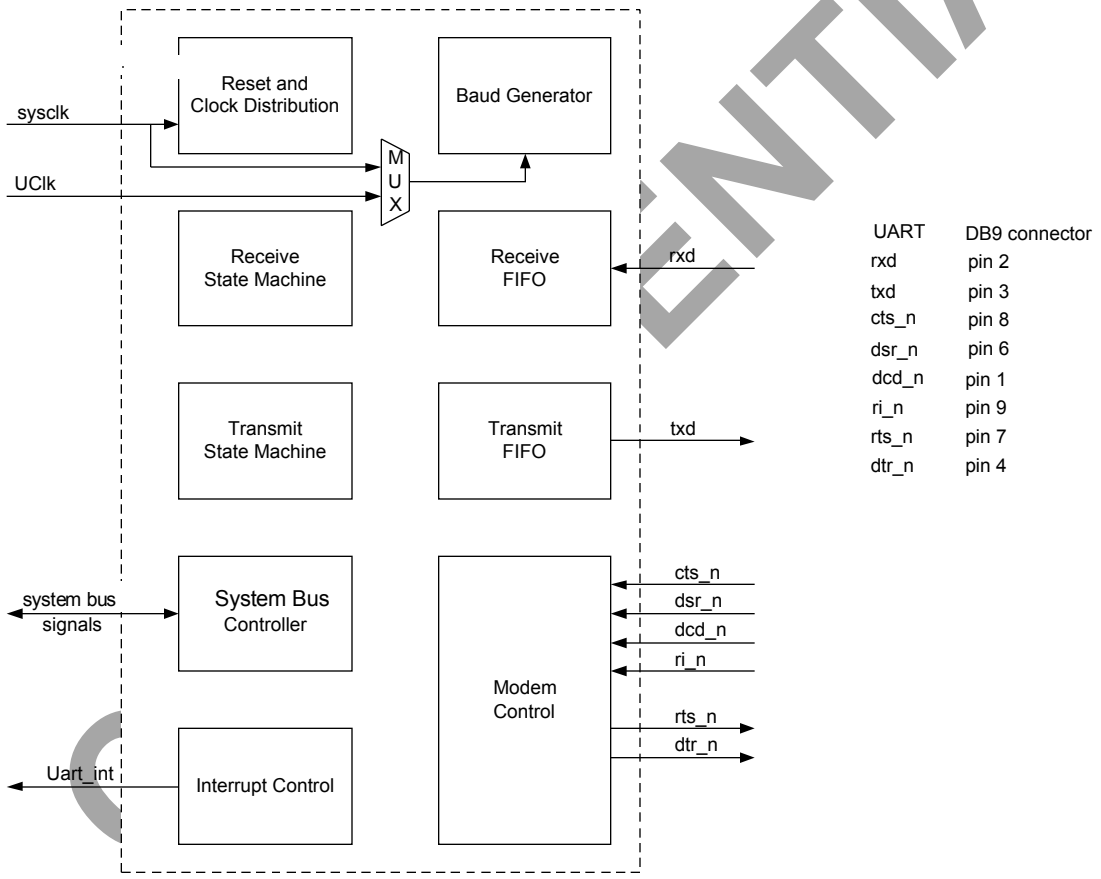

Figure 15. UART block diagram.

UART data formats

Baudrate = input clock frequency/(divisor x 16) = bits/second

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Bittime = 1/Baudrate = seconds/bit

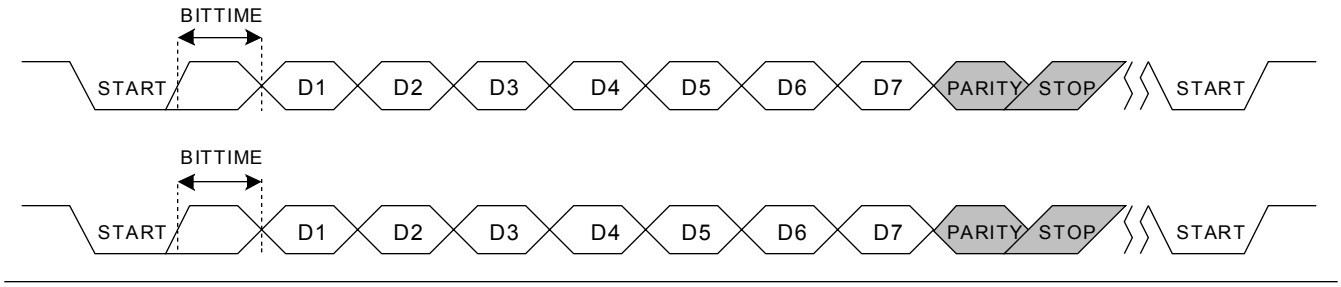

Figure 16. UART timing diagram.

Start bit

TXD and RXD are normally high. To transmit a character, drive the TXD line low for one bit time. The receiver always samples the RXD line; when it detects a start bit it starts shifting a new character in.

Data

A character can be programmed for 5-8 data bits. Both receiving and transmitting UARTs should be programmed for the same settings or communication fails.

Parity

Parity generation and checking can be enabled or disabled. If parity is disabled, no parity bit is transmitted and the receiver will not expect a parity bit. If parity is enabled, it can be even, odd, or stick parity.

- Even parity: Parity bit is '1' if the character has an odd number of 1's.
- Odd parity: Parity bit is '1' if the character has an even number of 1's.
- Stick parity: Parity bit can be forced to '1' or '0' .

Stop bit

Stop bits ('1') are the last bits to be transmitted/received for each character. The number of stop bits can be programmed to 1, 1 ½, or 2 Bittimes. Stop bits act as a spacer between characters when transmitted back to back. Program both receiving and transmitting UARTs for the same settings. Communication may fail if the number of stop bits expected by the receiver is greater than the number of stop bits actually received.

Break

A break is detected if the RXD line is held low longer than character time -- the time to transmit or receive a character including start, parity, and stop bits. This usually happens if the RXD line is disconnected or if the transmitting UART forced a break or is turned off. To force a break, set the break bit in the line control register. An interrupt is generated if a break is detected.

Modes

While only a few modes are standard, nearly limitless combinations are possible. Any of the following variables can be combined to create distinct modes:

- FIFO/non-FIFO
- Data bits
- Stop bits
- Parity

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I²C Master Controller

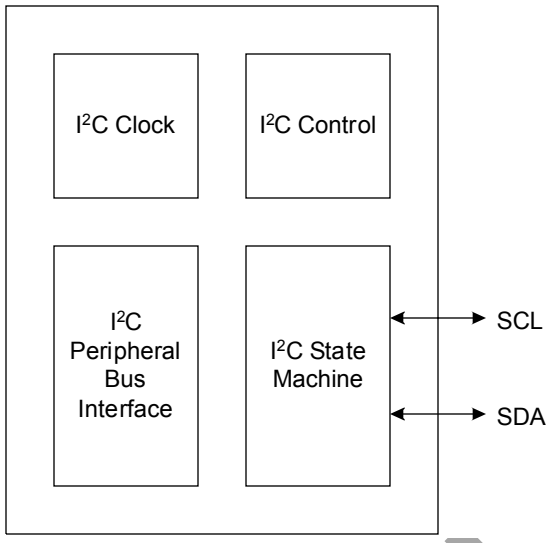

Figure 17. I²C master block diagram.

The I²C master is used to control external devices. It enables the Host CPU to access an external I²C slave device using a simplified register interface.

Stable data is received and transmitted through SDA while SCL is high. Changing the state of data on SDA is allowed only while SCL is low. The start signal, marked by the falling edge of SDA while SCL is high, informs all slave devices when initiating a data transfer sequence. In contrast, rising SDA signals stop while SCL is high. When the serial interface is inactive, the logic level of SDA and SCL are both high, due to external pull-up resistors.

The first data transferred after the start signal are the 7-bit slave address and R/W bit. When the R/W is high, the master reads from the slave registers. When R/W is low, the master writes to the slave registers. Features include:

- Programmable I²C bus clock rate
- Supports the Synchronous Inter Integrated Circuits (I²C) serial protocol
- Bi-directional data transfer
- Programmable address width up to 8 bits
- Sequential byte read or write capability
- Transmit both device and data addresses to perform device, page and address selections for read and write tasks
- Interrupt generation when byte received or byte transmitted

I²C write

This function sends device address and Write data. It requires bytecount, device address and data before beginning transfers.

I²C read

This function sends device address and reads data. It requires bytecount and device address, and reads value(s) from the register.

I²C operations

First, software will configure the I²C controller by programming the CONFIG register and selecting the proper CLKDIV register value.

Then software may program the device address register DEVADR with an address and/or data to be written to or read from the external I²C slave device. To access an external I²C slave device the CPU should program the DEVADR register and / or ADR/DATAOUT registers. To do a burst read or a burst write the BYTECNT register needs to be set as well.

The direction and the start of the transfer is determined by the RWDIR bit in the STARTXFER register. Writing the RWDIR bit starts the I^2C state machine. It will handle all proper hardware signalling.

The state machine starts by asserting a start condition on the I^2C bus, followed by shifting seven bits contained in the DEVADR register. It then checks for an acknowledge signal from the addressed slave device. If there is no acknowledge the ACKERRDET bit is set in the I^2C STATUS register.

In case the ADRDIS bit was set to '0' the state machine will take the data from the ADR register.

Then in case of a write it will shift out the eight bits in the DATAOUT register OR in case of a read it will shift data into the DATAIN register.

The I^2C bus consists of two bi-directional lines the Serial Data (SDA) line, and the Serial Clock (SCL) line. A start condition on the I^2C bus is indicated by asserting SDA low while SCL high.

Subsequent device address and data is shifted one bit per SCL.

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I²C Slave

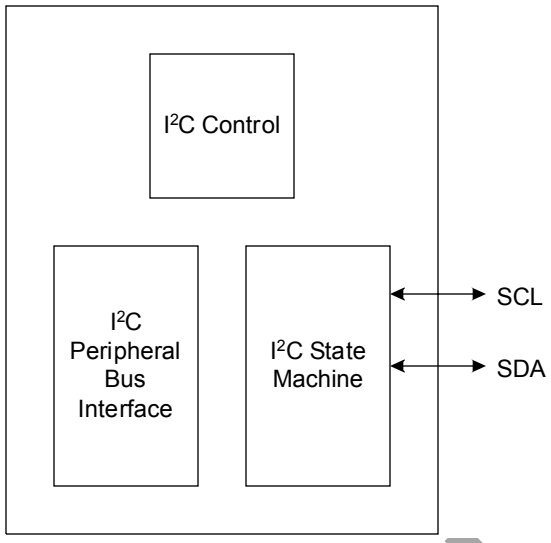

Figure 18. I²C slave block diagram.

When configured as a slave device, the EM8550 can receive data from an external device. The difference between I²C slave and I²C master is that the latter acts as the controller while the I²C slave only receives information. The I²C master and slave blocks use separate SCL and SDA pins.

The EM8550 supports the Synchronous Inter Integrated Circuits (I²C) serial protocol with bi-directional data transfer and up to an 8-bit programmable address width. It handles sequential byte reads and writes, up to 64 bytes long. Device and register addresses can both be transmitted to the device for page and address selection to perform read and write accesses. It generates interrupts when a byte is received or needs to be transmitted.

Two pins control the operation of the 2-wire-bus.

- SDA: the bi-directional open-drain serial data IO.
- SCL: the serial interface input clock controlled by the external I²C master.

EM8550 acts as a slave device; use the ADDR_REG[7:0] register to select the 7-bit slave address.

Stable data is received and transmitted through SDA while SCL is high. Changing the data on SDA is only allowed while SCL is low. The start signal, marked by the falling edge of SDA while SCL is high, alerts all slave devices that a data transfer sequence has been intiated. In contrast, rising SDA signals a STOP while SCL is high. When the serial interface is inactive, the logic levels of SDA and SCL are both high due to external pull-up resistors.

If the transmitted slave address matches the address programmed by ADDR_CTRL, EM8550 acknowledges selection by bringing SDA low on the ninth pulse of SCL clock (ACK cycle). Otherwise, SDA and SCL remain high; EM8550 does not acknowledge its presence.

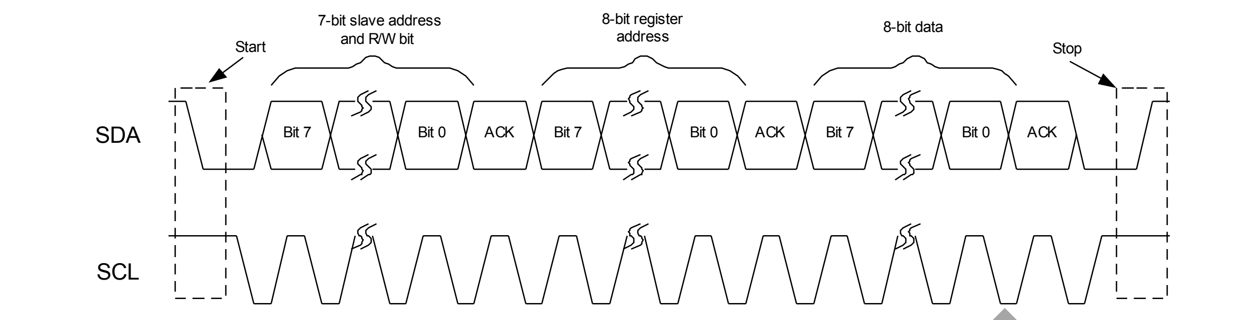

Figure 19. I^{2}C transfer timing diagram.

Read and Write from EM8550

<table>
<tr><td>S(1)</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>R/W=0(2)</td><td>A</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>A(3)</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>A</td><td>STOP</td></tr>
<tr><td colspan="8">7-bit slave address</td><td></td><td colspan="9">8-bit data</td><td></td><td colspan="9">8-bit data</td><td></td></tr>
</table>

1. S means START.
2. R/W=0 means Master writes to slave; R/W=1 means Master reads from slave.
3. A means ACKNOWLEDGE

Local Peripheral Bus Interface

The EM8550 contains a Local Peripheral Bus (LPB) interface to which a variety of external components can be connected. The interface supports a generic, 16-bit, multiplexed address/data interface adaptable to a wide range of devices. The bus defines an external address space of 64K words (128K bytes). Only a single address space is defined - no distinction is made between I/O and memory spaces, for example. The LPB is implemented as a state machine which is clocked at the system clock frequency (81 MHz nominal). Thus all transfer cycle timing parameters occur in multiples of the system clock period (12.3 ns nominal).

The EM8550 is the LPB bus master at all times. The EM8550 internal RISC CPU can initiate either single transfer read/write cycles, or burst mode read/write transactions. Burst mode transactions are useful for moving bulk data when an external device is equipped with FIFO's . They consist of an initial address cycle, followed by a sequence of up to 32767 data transfers.

The LPB interface always transfers 16-bit values. It does not support byte-lane enables, but may be configured to swap bytes during read and write transfers. Also, when operating in single-transfer mode, an option exists to automatically increment the address value after each cycle.

An LPB_Reset signal is provided as an output to allow the EM8550 to reset attached devices. The interface includes support for pseudo-DMA operation, interrupts, and four programmable I/O pins

Pseudo-DMA operation

Attached devices which are capable of supporting burst mode data transfers (i.e., they contain FIFO's in the read/write data paths) may signal their requirement to read or write data by asserting the LPB_INTR signal. The EM8550 RISC CPU can then initiate a burst read or write transfer upon recognizing the active INTR signal. The transfer will continue until the transfer count internal register decrements to zero. This is referred to as pseudo-DMA operation since the EM8550 continues to operate as bus master at all times.

Programmable I/O

Four general purpose programmable I/O pins (LPB_PGIO[3:0]) are associated with the LPB interface. Each pin may be separately configured as input or output, and when configured as inputs, the polarity of the latched values may be optionally inverted relative to the pins.

DTACK/RDY# Sampling

The DTACK/RDY# signal is asserted by the addressed device to terminate the current transfer. DTACK/RDY# is assumed to be an asynchronous input, and therefore is synchronized internally to the system clock. The DTACK/RDY# signal must be sampled high for one or more system clocks, then sampled low for one or more system clocks, and finally sampled high in order to complete the bus transaction. Due to the internal sampling, the DTACK/RDY# low period must be greater than the system clock period to guarantee it is recognized. In the event no valid DTACK/RDY# is asserted, the bus cycle will "time out" after 65,536 system clock periods.

Timing Diagrams

The figures below show the functional characteristics of the single-cycle and burst transactions. The boxed “x” notation in the timing diagrams indicates the time differential between indicated events expressed as x periods of the internal system clock.

The circled “x” notation indicates a time differential between events of which one is internally synchronized by the system clock. Therefore, the value x represents the minimum value, but may be up to one system clock period greater.

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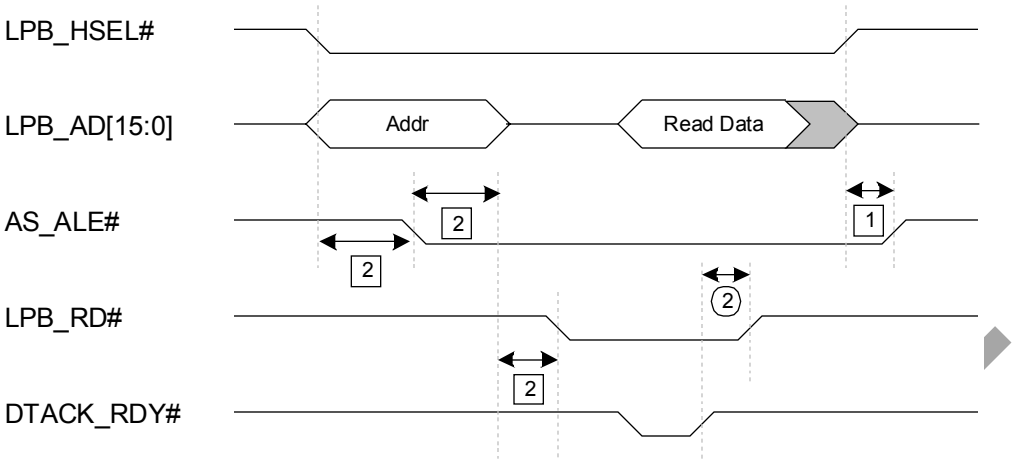

Figure 20. LPB single cycle read timing diagram.

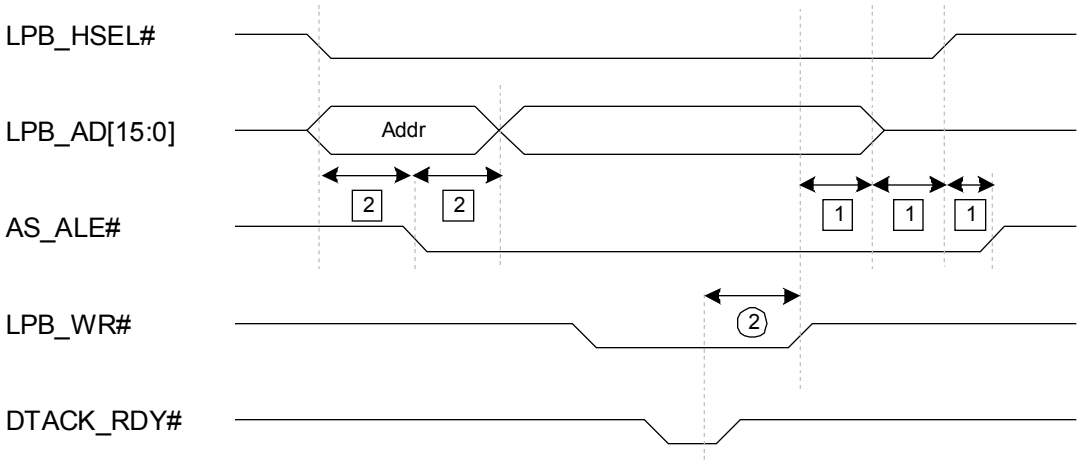

Figure 21. LPB single cycle write timing diagram.

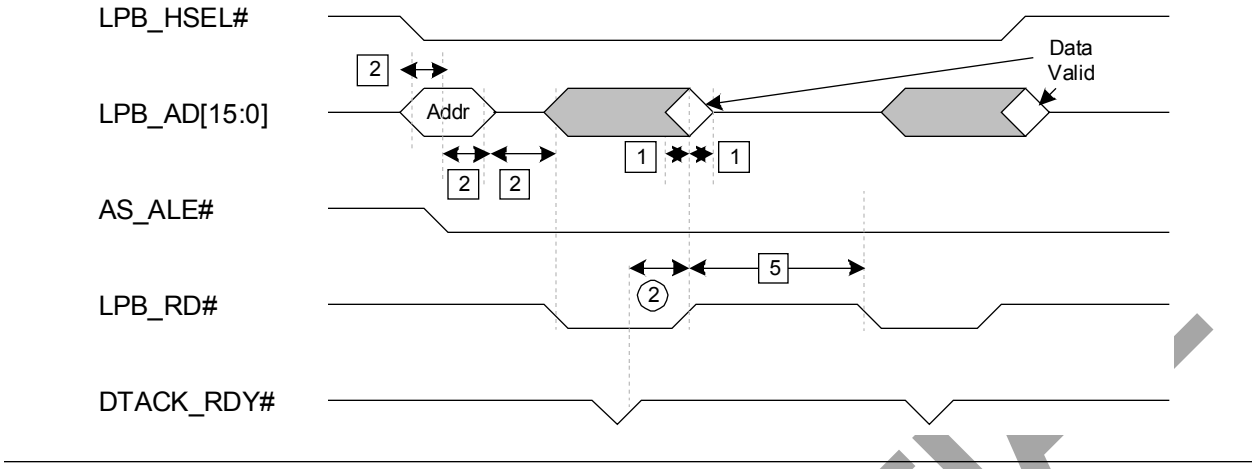

Figure 22. LPB burst read timing diagram.

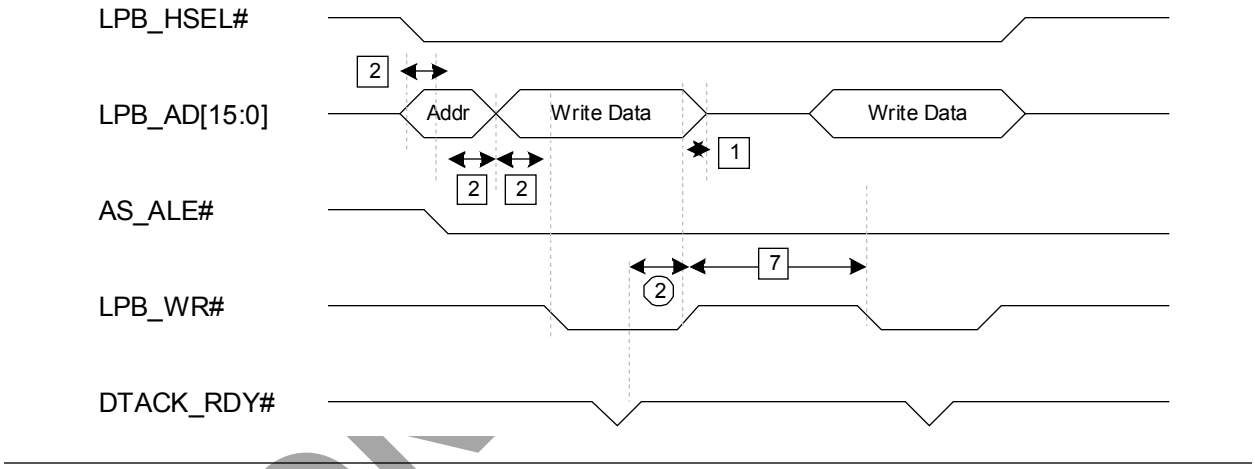

Figure 23. LPB burst write timing diagram.

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General Purpose I/O Controller

The GPIO Controller consists of two sub-blocks, PIO0 and PIO1, which together provide 32 bits of general purpose IO pins. The PIO1 interface shares pins with the SPI (See “Synchronous Parallel Interface (SPI)” on page 41.). While PIO1 is active, the SPI is inactive, and vice-versa.

The GPIO is a bidirectional 32-bit wide interface that can connect with external devices. The controller has 32 independently programmable pins. Each pin can be programmed as an input or output, possesses independent polarity controls, and supports an edge detect interrupt for input transitions.

Independent level-sensitive I/O

Set any of the 32 pins to either input or output using firmware. In output mode, the pins may be set to a high or low voltage. Each bit has independent polarity control to keep pin voltage independent of logical signal level.

PIO interrupt

An interrupt may be generated when any input-only pin transitions from a low to high state or vice versa with respect to the polarity flag. This interrupt is useful if PIO events are infrequent or unpredictable (such as from a keypad or remote control keypress). Mask the interrupt in the interrupt controller if it is not needed.

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IDE Controller

This block shares pins with the DVD loader interface (See "DVD Loader Interface" on page 36.). While the IDE controller is active, the DVD loader interface is inactive, and vice-versa. The IDE controller gets data from the IDE drive and sends it to the MAC. The IDE interface is primarily used to connect mass storage peripherals to the system. The flexible, low-cost ATA interface is a standard addition to consumer-level DVD drives. The EM8550 provides a glueless interface to these IDE/ATAPI drives. ATA drives are memory-mapped devices.

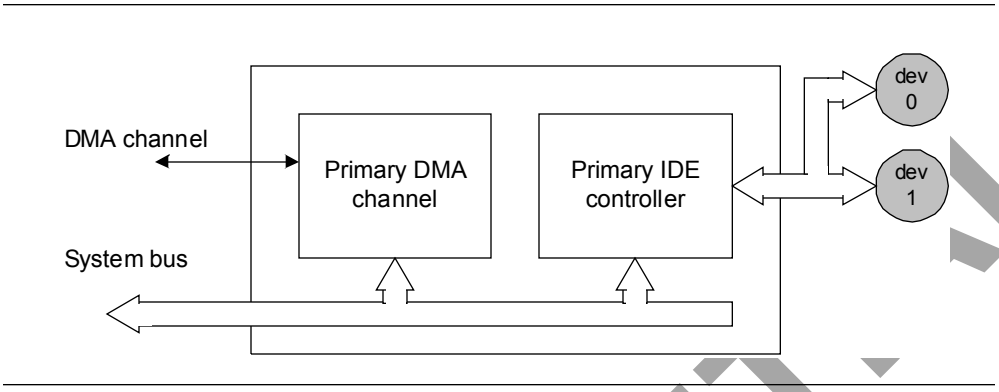

Figure 24. IDE controller block diagram.

IDE interface

The pre-fetch and post write sub-module controls data read/write of external ATA/ATAPI devices during read sectors, write sectors, read multiple and write multiple commands. When both data pre-fetching and posting are enabled, accesses to the IDE data port use the FIFO in the DMA channels.

Data is pre-fetched on 512 bytes boundaries into the FIFO during data port reads; data is written into the FIFO during data port writes. During read command data transfers, writes to any register in the external ATA/ATAPI device other than the data port will cause the FIFO to be cleared and pre-fetched data to be lost. During write commands with write posting enabled, a write to any register other than the data port register causes data in the FIFO to be flushed to the external device before the write can continue.

DMA mode

The DMA channel interfaces to the MAC controller (See "Memory Access Controller (MAC)" on page 13.) and an IDE controller (See "IDE Controller" on page 33.). The IDE controller block strobes data into and out of the 64x32 bit FIFO in the DMA channel block based on the setting of the read/write direction bit. These channels contain the Bus Master and IDE Control registers mapped to I/O space.

A physical region descriptor (PRD) describes the physical memory region to be transferred. Each PRD entry is 8 bytes long. The first 4 bytes specify the byte address of a physical memory region. The next two bytes specify the region count in bytes (64K byte limit per region). A value of zero in these two bytes indicates 64K. Bit 7 of the last byte indicates the end of the table. Align the descriptor table on a 4- byte boundary; the table cannot cross a 64KB boundary in memory.

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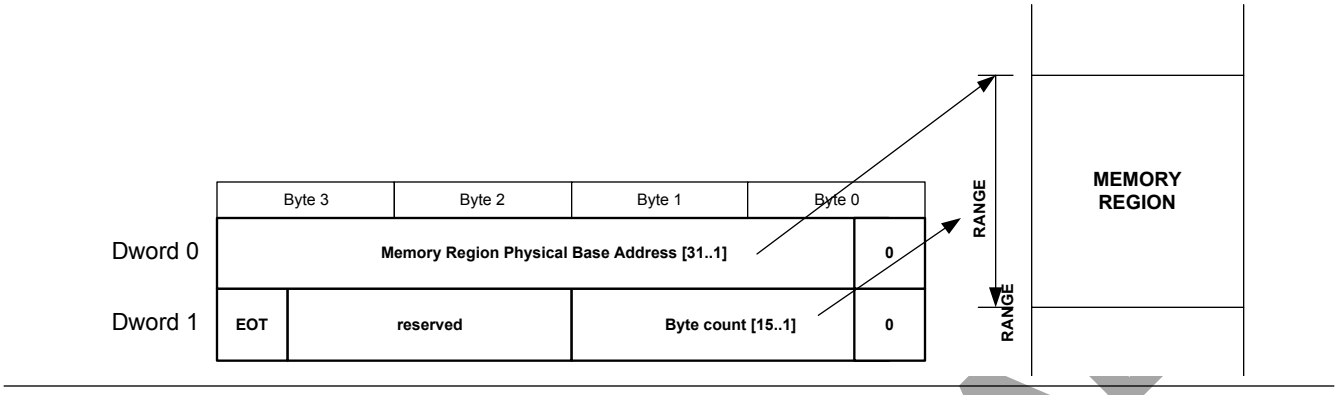

Figure 25. Physical region descriptor table entry.

IDE mode support

PIO modes

PIO, or Programmed Input/Output, is an established ATA device communications standard. There are five different PIO modes, each with different transfer rates. Higher mode numbers indicate higher transfer rates. All PIO modes use the CPU to transfer data, making this method unsuitable for multitasking environments. PIO has recently taken a back seat to DMA modes.

DMA modes

DMA, or Direct Memory Access, is used when a peripheral device bypasses the CPU and transfers data directly to or from memory. DMA is currently the best way to transfer data from hard drives to memory since most modern operating systems assign the CPU to more important tasks. Initially, DMA modes were not widely adopted, but they became commonplace with the advent of Ultra DMA mode. When compared to single- and multi-word transfers, Ultra DMA effectively doubled bandwidth by clocking data twice per clock cyle. Ultra DMA mode 2, also called UltraDMA/33 is used pervasively today.

ATA-1 standard

The ATA-1 specification, defined as an ANSI standard in 1994, eliminated some major compatibility problems with the early ATA/IDE drives. Prior to the ATA-1, conflicts frequently arose when drives produced by different manufacturers were placed as master and slave on the same channel.

The original ATA/IDE standard supported one or two hard drives on the same bus. One was configured as master and the other as slave. It also supported the following modes:

- PIO modes 0, 1 and 2
- DMA mode 0, 1 and 2
- Multiword DMA mode 0

ATA-2 standard

As technology improved, there arose a need for faster transfer rates and enhanced features. In 1996 the ATA-2 standard was defined as an ANSI standard backward compatible with ATA-1. It included support for the following features:

- Faster PIO modes: 3 and 4.
- Faster DMA modes: 1 and 2
- The "Identify Drive" command (also called Plug 'n' Play), which allowed software to query the drive for its geometry and characteristics.

Several manufacturers marketed ATA-2-based drives under different names like "Fast-ATA", "Fast-ATA-2" and "Enhanced IDE". None of these were actually separate standards.

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ATA-3 standard

In 1997 the ATA-3 ANSI standard improved the reliability of the faster transfer modes introduced with ATA-2. It also added SMART, the open standard for monitoring disk drive health. Visit <http://www.quantum.com/src/whitepapers/smart/contents.html> for details.

ATA/ATAPI-4 standard

The ATA/ATAPI-4 standard recently added some significant and long-awaited features:

- ATAPI (AT Attachment Packet Interface) for devices such as CD-ROMs and CD-Rs that required commands not present in the preexisting ATA standard
- Removable media (Zip drive)
- Overlapped feature set allowing devices that required extended time to perform a bus release so that other devices on the bus could be used
- Ultra DMA data transfer protocol, also called Ultra ATA, which clocked data twice per clock cycle by using both the negative and positive transition
- Definition for an optional 80 conductor cable to be used for Ultra ATA devices

DVD Loader Interface

This block shares pins with the IDE controller interface (See "IDE Controller" on page 33.). While the DVD loader interface is active, the IDE controller is inactive, and vice-versa. The DVD loader interface module communicates with the external DVD loader through two channels:

- An 8-bit A/V channel that transfers audio and video data from the loader to the DVD loader interface and to hostmem via DMA.
- Serial Host IF channel that transfers commands from EM8550 to the loader, and status/information from the loader to EM8550. The module has two sets of registers that control the operation of EM8550's audio/video interface and Host interface.

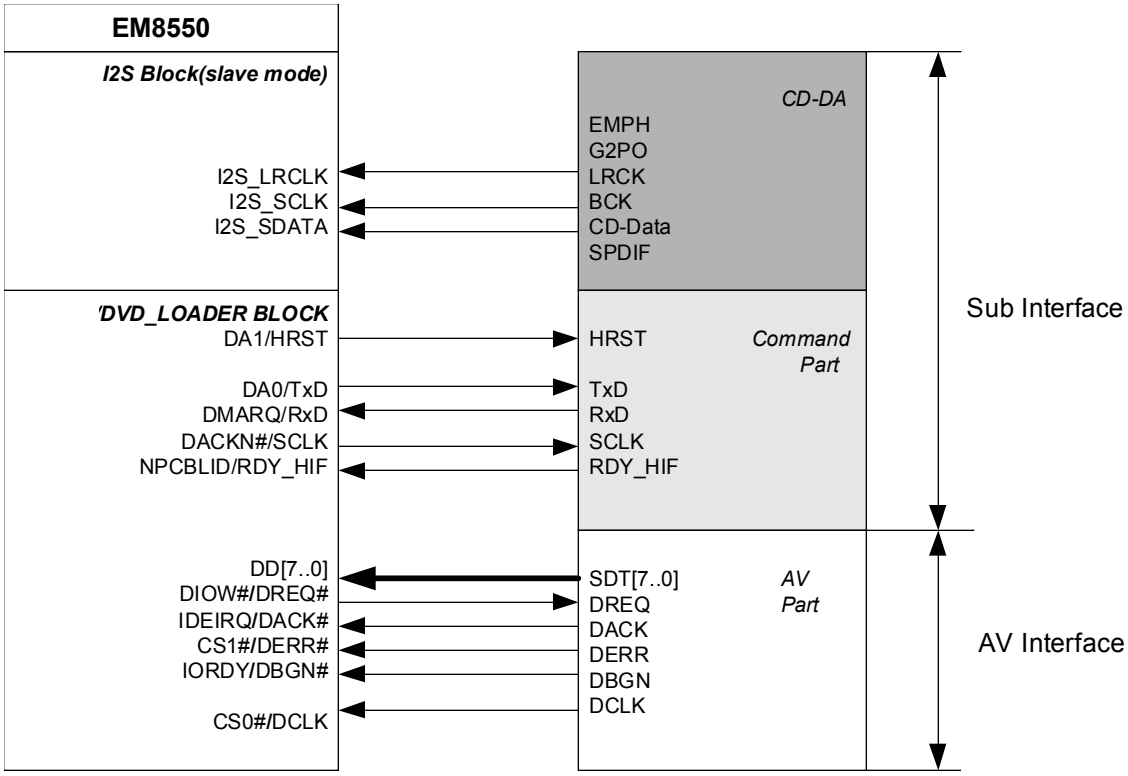

Figure 26. EM8550 and DVD loader interface.

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I²S Block (Master or Slave Mode)

The I²S bus can transfer bandwidth-intensive information such as uncompressed audio and video. The interface receives information from any I²S-compliant transmitter.

Receiver (EM8550) slave.
SCLK, LRCLK, SDATA are inputs to I²S block.

Receiver (EM8550) Master.
SCLK, LRCLK are outputs from I²S block.
SDATA is input to I²S block.

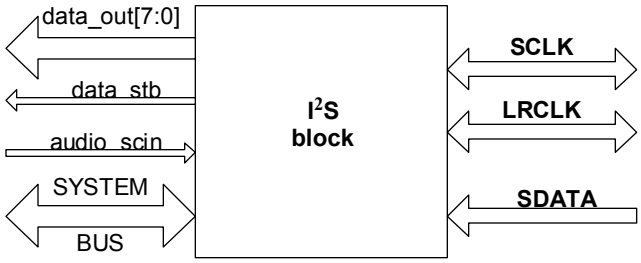


Figure 27. I²S block diagram.

The I²S block can be programmed to function as a slave or master device.

In slave mode (maximum bandwidth = 20 Mbps), the external transmitter is the master and SCLK, LRCLK, SDATA are EM8500 inputs. These signals are synchronized to the external clock on the transmitter side.

In master mode (maximum bandwidth = 20 Mbps), the external transmitter is slaved to the SCLK, LRCLK signals generated by EM8500 and synchronized with the external SCIN clock. The SDATA signal, an EM8500 input, provides data synchronized with SCLK and LRCLK.

In both modes the data is always accepted as MSB first/high bytes first. The I²S block need not know the quantity of bits transmitted. If the *length* of the number of the transmitted bits is unknown, then the I²S block recovers all bits in the left and right frame and forwards them to the DMA block. If the I²S block receives fewer bits (SCLK clocks) than those specified by a known length, the received data is truncated to the value specified in the length register (least significant bits are sets to zero). If the I²S block receives a more bits (SCLK clocks) than specified by a known length, only the specified number of bits is forwarded to DMA channel; the remainder is dropped.

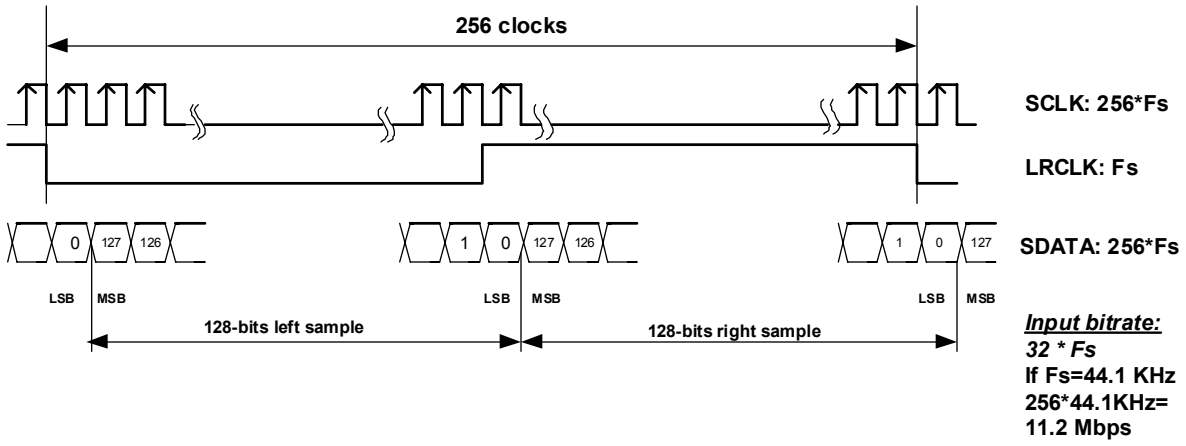
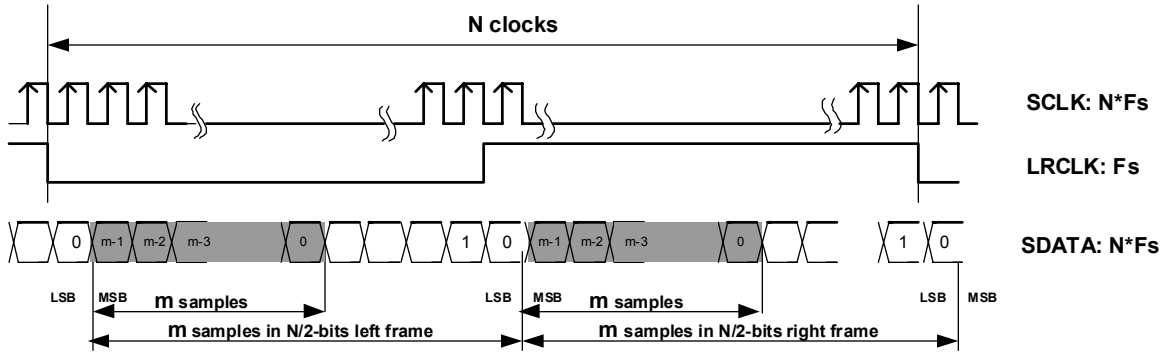


Figure 28. I²S timing diagram (256Fs 128-bit).



Each frame has N/2 samples.
Only M of them are accepted.

Figure 29. I²S timing diagram (N*Fs m-bits slave mode).

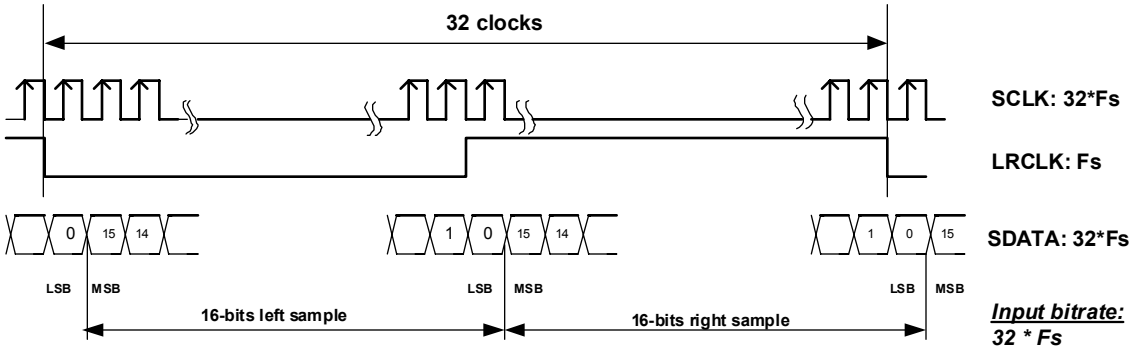


Figure 30. I²S timing diagram (32Fs 16-bits).

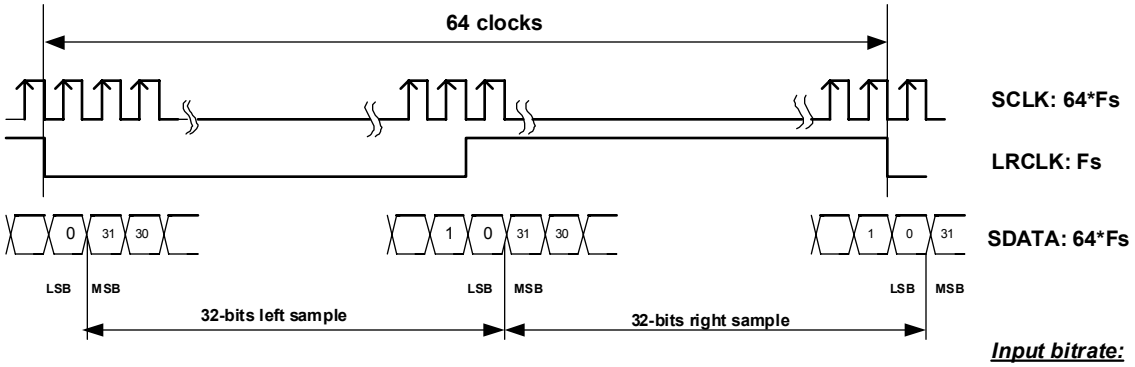


Figure 31. I²S timing diagram (64Fs 32-bits).

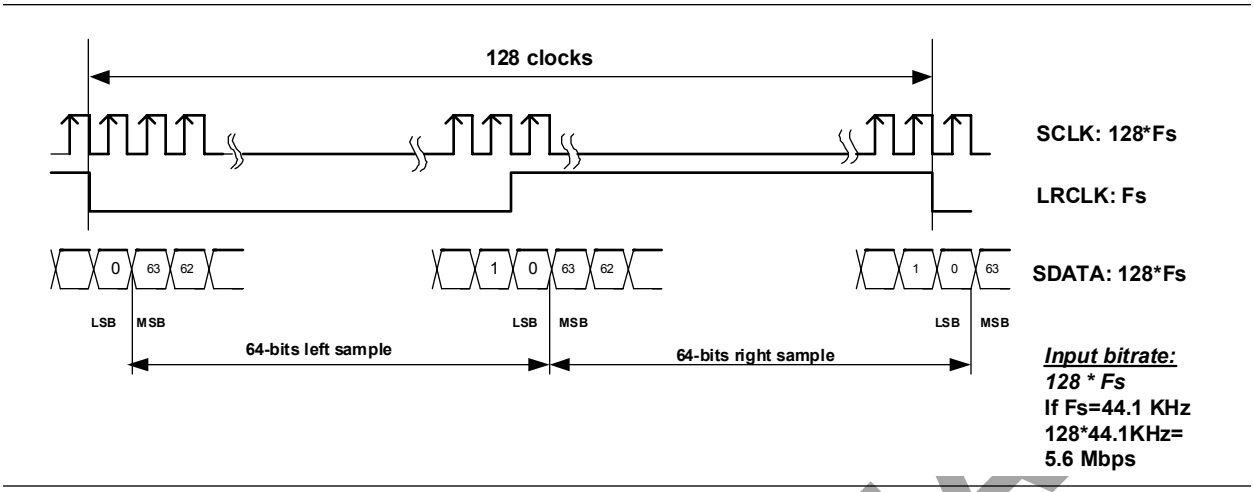


Figure 32. I²S timing diagram (128Fs 64-bits).

Synchronous Parallel Interface (SPI)

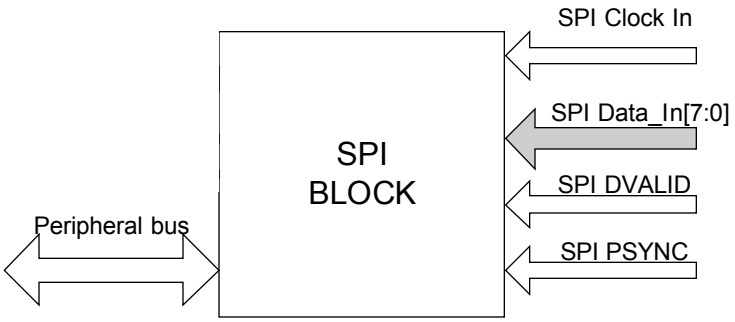


Figure 33. SPI block diagram.

The SPI block shares pins with the GPIO block (See "General Purpose I/O Controller" on page 32.). While the SPI block is active, PIO1 of the GPIO block is inactive, and vice-versa. The SPI block accepts compressed video data from a external device through the SPI interface described in the DVD Document A010. It is commonly used for broadband applications in which a single channel of multiplexed data is selected and sent to a decoder. Eight bits of Data In are synchronous to the Clock In signal. DVALID high indicates valid data; otherwise data is ignored.

One packet of data contains either 188 or 204 bytes. The header sync byte value (i.e. the SPI data byte received along with SPI_DVALID=1 and SPI_PSYNC=1) of each 188-byte packet is 0x47 or for a 204 byte packet either 0x47 or 0xB8.

The maximum allowed bandwidth through SPI is 20 Mbit/s.

This block enables the count of corrupted packets received during transmission. Sync packet errors and size packet errors are recognized and counted.

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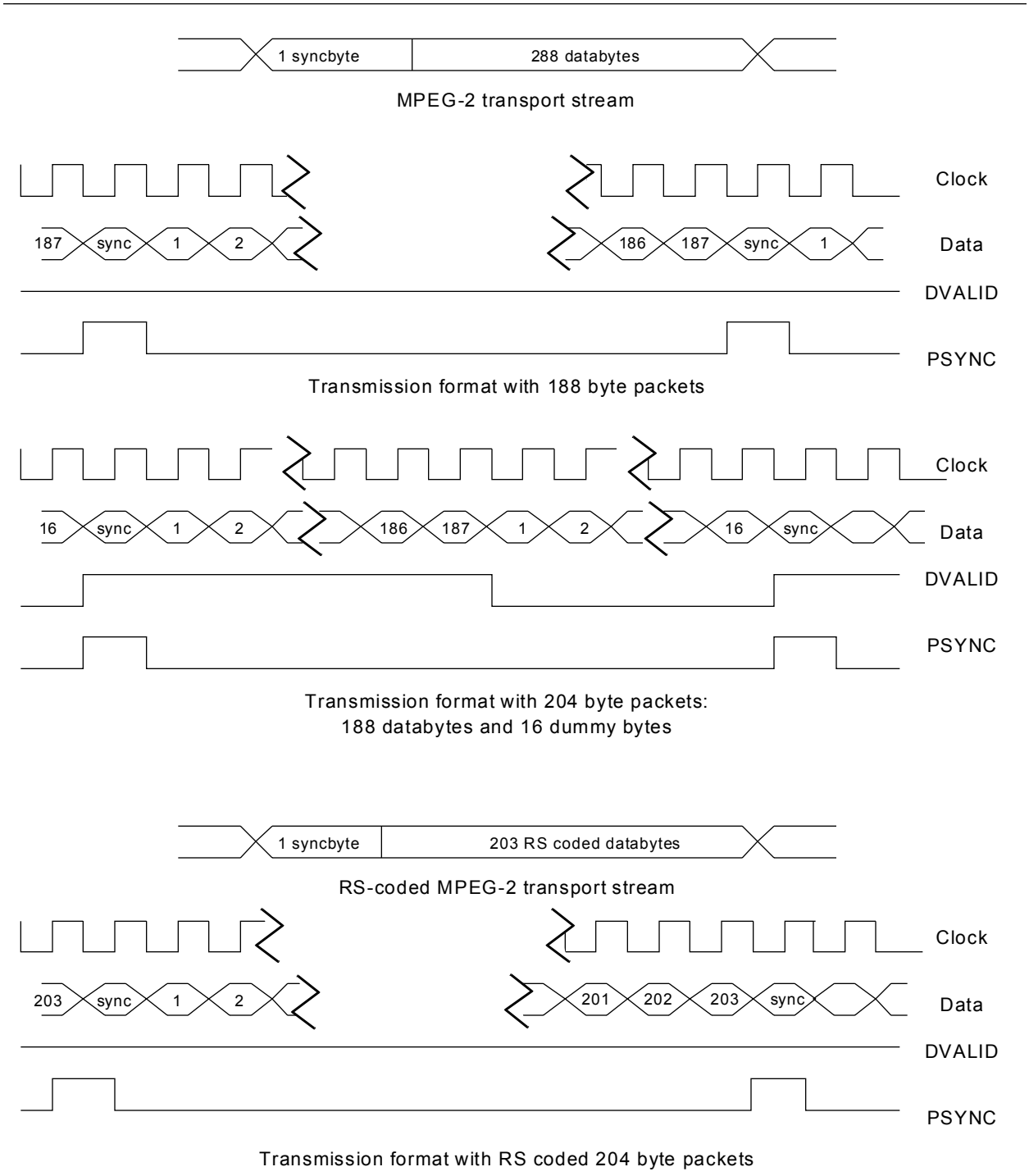

Figure 34. SPI timing diagrams.

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SPI/I^{2}S DMA

The DMA transfers the information from the source (I^{2}S or SPI block) to the destination address (Memory Access Controller). The SPI/I^{2}S DMA, like other DMAs, needs the destination address and the byte count designating the number of bytes to be transferred.

The maximum bandwidth of SPI/I^{2}S DMA block is 20 Mbps. SPI/I^{2}S devices may send data through the DMA channel which must always accept data; it cannot slow down or drop data coming from the SPI or I^{2}S block. The SPI/I^{2}S DMA block may automatically support circular buffer structure in the host SDRAM and may issue an interrupt regarding the fullness of that circular buffer. Software must prevent buffer overflow by servicing corresponding interrupt service routines. For buffer overflow, the SPI/I^{2}S block issues the corresponding interrupt, if enabled, and overwrites data in the circular buffer.

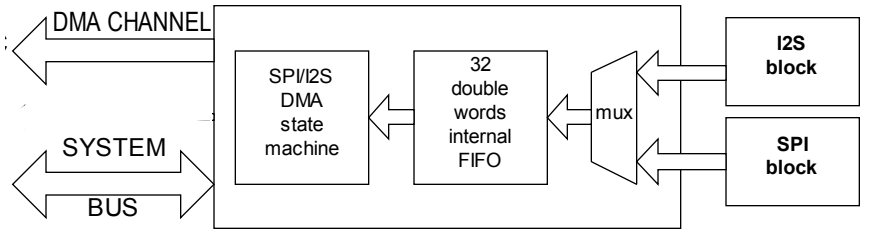

Fig.1 SPI/I2S DMA block

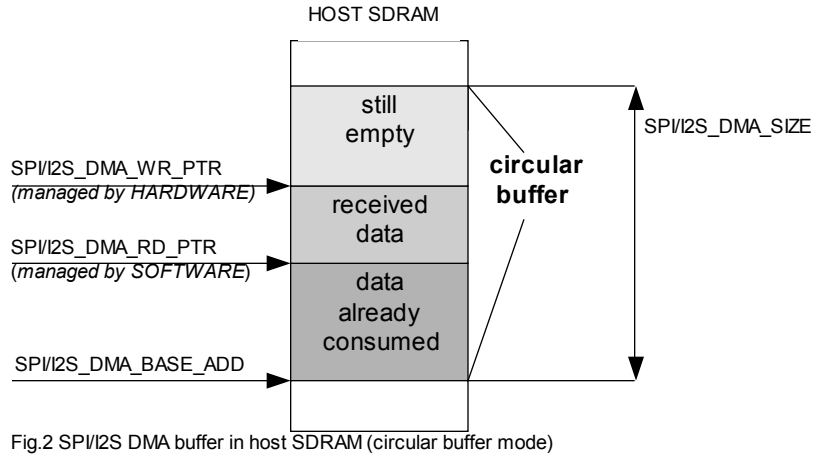

Fig.2 SPI/I2S DMA buffer in host SDRAM (circular buffer mode)

Figure 35. SPI/I^{2}S DMA architecture and operation.

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Vacuum Fluorescent Display Controller Interface

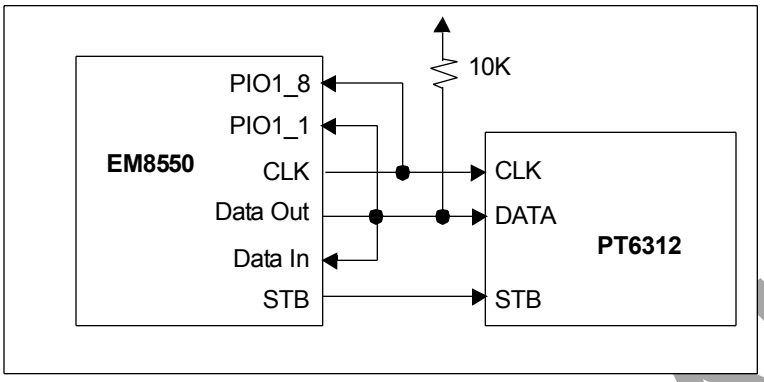

Figure 36. VFD block diagram.

This block programs a VFD controller chip such as the NEC µPD161311 or PT6312 via a glueless interface. Supported functions include:

- VFD display port control
- Key scanning functions
- LED port control
- Full configuration of controller chip

It supports either the 4wire protocol (Din, Dout, clock, strobe) or the 3wire protocol in which Din is connected to Dout (i.e., external pullups are required).

Video

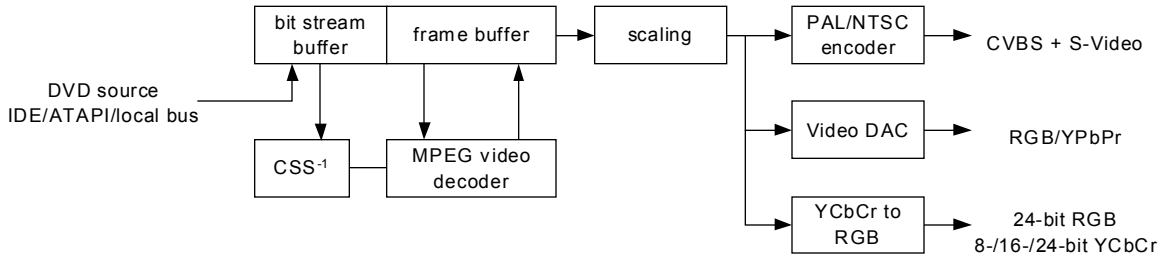

Figure 37. Video pipeline diagram.

Video Processing

Sub-pictures

Sub-pictures work only for DVD playback. These compressed bit maps are overlaid on decoded MPEG video. Subpictures can be scrolled up and down and faded in and out. The area, content, color, and contrast in every video field can be changed, enabling (for example) highlighting effects.

OSD (on-screen display)

The OSD enables simple full screen graphical menus to be displayed and blended with the MPEG decoded video and sub-picture. The EM8550 scales and displays OSD pictures using bilinear horizontal and vertical filters. It supports 4 palletized color depths: 4 colors (2 bits per pixel), 16 colors (4 bits per pixel), 128 colors (7 bits per pixel), and 256 colors (8 bits per pixel). The bit map can be compressed using Run-Length Coding (RLC) in 2, 4, and 7-bit per pixel modes. A 256 x 32 Color Look-Up Table (CLUT) is provided to convert the 2, 4, 7, or 8-bit code into a 24-bit YCbCr color and 16 levels of alpha blending. The Highlight function is supported in 2, 4, and 7-bit per pixel modes.

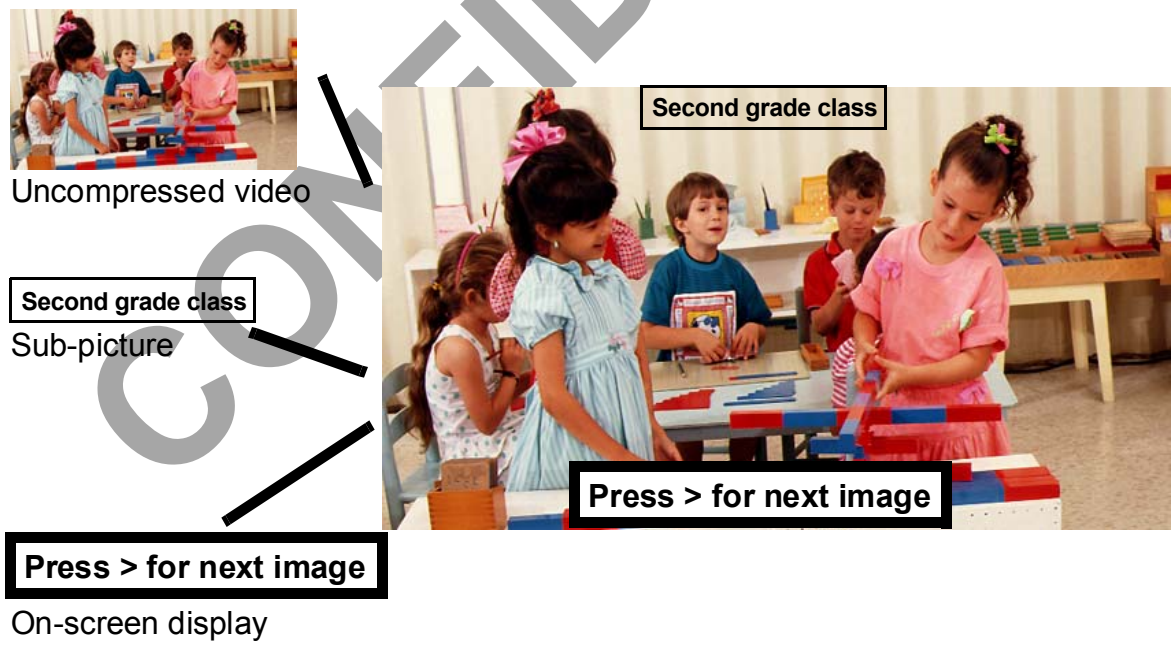

Figure 38. Video processing engine.

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Letter box display

This provides vertical downscaling, enabling 16:9 pictures to be displayed in a letterbox fashion on a traditional 4:3 display.

Pan and scan display

In this mode, the video image can be expanded to 16:9 and a section of the image can be displayed at full height on a 4:3 TV display.

Alpha blending

This provides two layers of blending: the sub-picture over the MPEG video and the OSD over both the sub-picture and MPEG video. The are 16 levels of blending.

MPEG Engine

The MPEG video decoder engine contains the following modules used for MPEG-1, MPEG-2, and MPEG-4 advanced simple profile video decoding (without GMC and QPEL):

Huffman Decoder

The MPEG video decoder engine uses the Huffman Decoder as its front end. Under direct commands from the RISC processor, the Huffman Decoder extracts fixed-length, variable-length, or start codes from the bitstream and returns the value to the RISC processor or passes them directly to the Inverse Quantizer.

Inverse quantizer

The Inverse Quantizer block resides between the AC/DC predictor block and the inverse DCT block. Its primary function is to convey coefficients from the AC/DC predictor through the quantization matrix to the Inverse Discrete Cosine Transform module. It supports the MPEG-1, MPEG-2 MP@ML, and MPEG-4 advanced simple profile.

Inverse DCT

The IDCT (Inverse Discrete Cosine Transform) module is a hardware implementation of the DCT/IDCT of an 8×8 pixel block used in MPEG compression/ decompression. The DCT transforms a block of 8×8 pixels into a block of 8×8 transformed coefficients. The IDCT converts the block of 8×8 transformed coefficients back into pixels (or pixel differences for non-intra pictures), which are sent to the Motion Compensation block.

Motion compensation

The Motion Compensation Module performs all the motion compensation tasks required to decode MPEG-1, MPEG-2, and MPEG-4 bitstreams. This includes predicting the image block for the picture being decoded, using pixels from previously decoded pictures.

AC/DC predictor

If the input stream is MPEG-1 or MPEG-2, the AC/DC predictor passes through. Otherwise, it receives data from the zigzag and outputs it to the inverse quantizer. This module supports MPEG-4 advanced simple profile.

I, P, B, GOP

The video decoder accommodates three types of coded frames -- I, P, B -- as well as groups of pictures (GOPs), which are a series of frames that help enable random accessing and editing. I frames are coded as standalone still images, and allow random access points within the video stream. P frames use motion compensation to provide more compression than I frames, and serve as a reference for B and future P frames. B frames, which provide the most compression and noise reduction, produce bi-directional prediction using the closest past and future I or P frames as references.

Video Outputs

The EM8550 display controller reads picture data from the DRAM and displays it with proper format, timing and synchronization signals. It is a real-time process driven by the video clock.

The display controller operates in one of four modes:

- Master mode, in which the display controller generates HSYNC and VSYNC from an internal or external video clock up to 80 MHz
- Slave mode, in which the display controller receives HSYNC and VSYNC from an internal or external video clock up to 80 MHz

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To adapt the source type to the display device type, two different display modes are implemented (Table 5, "Display modes based on source and display device types.," on page 47).

Table 5. Display modes based on source and display device types.

	Source Type	Display Device Type	Display Mode
1	Progressive	Progressive	Frame-Based
2	Progressive	Interlaced	Field-Based
3	Interlaced	Progressive	Field-Based
4	Interlaced	Interlaced	Field-Based

The source type is derived from the sequence extension and the picture coding extension of the MPEG video stream. The video display timing for both interlaced or non-interlaced (progressive) video output can be set as high as 120 Hz. Picture scaling (when necessary) is performed according to the display mode. In case 3 for example (interlaced source, progressive display device), up-scaling is performed on a field base.

Slave/master modes

The video outputs operate as either a timing master, CCIR601 slave, or CCIR656 slave. The CCIR601 and CCIR656 slave modes are highly configurable. The CCIR601 slave mode can be configured for rising or falling edges for HSYNC/VSYNC, and for VSYNC vertical synchronization or field vertical synchronization. The video outputs do, however, operate as a slave to the active video area of the display. Encoding is possible on VBI lines, except for those lines used for built-in WSS, CGMS, and closed captioning.

Digital video output

The digital video output interface can be programmed to output 8-/16-bit CCIR601 or 8-/16-bit CCIR656 4:2:2 YCbCr data. It may be operated as a timing master or slave. An additional 24-bit RGB output mode is also supported.

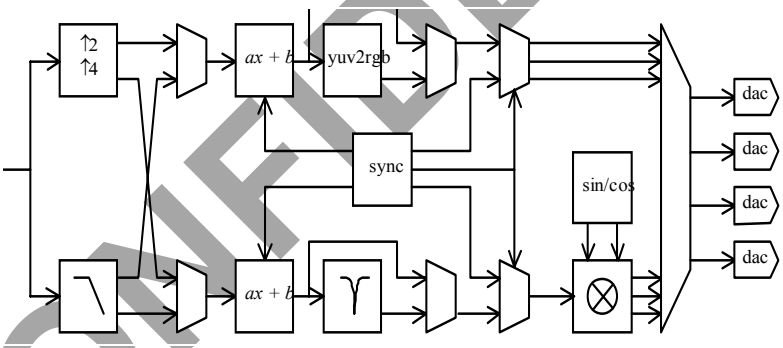

Figure 39. EM8550 TV encoder path block diagram.

Scaler

The EM8550 performs horizontal and vertical up/down-sampling of the video using high-quality 4-tap filters. The scaling ratios are arbitrary and allow scaling up DVD format to high-resolution HDTV.

DVI interface

The EM8550 directly interfaces with a DVI transmitter through its 24-bit RGB interface. The interface sends uncompressed digital video to the display device.

Composite and S-video outputs

EM8550 includes a high-quality NTSC/PAL encoder (with optional Macrovision v7.1 protection) that supports the NTSC-M, NTSC-J, PAL-B/D/G/H/I, PAL-60 and PAL-M baseband video standards. It features three 10-bit video DACs that generate simultaneous composite and s-video outputs. The analog video outputs are capable of driving a doubly-terminated 75-ohm load.

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Component analog output

The EM8550 also includes component YPbPr or RGB analog outputs, with optional Macrovision AGC v1.03 protection in 480p YPbPr mode. Component analog output can be programmed as either RGB or YPbPr video data, interlaced or progressive, and from NTSC/PAL resolutions up to 1600x1200P or 1920x1080i. The analog video outputs are capable of driving a double-terminated 75-ohm load or single-terminated load for minimum power consumption.

When generating analog RGB or YPbPr video, the composite video output is always present; s-video output is unvailable.

Supported analog formats are:

- RGB and composite video for SCART support
- RGB with sync on green
- SMPTE GBR
- Betacam YUV
- M-II YUV
- SMPTE YPbPr

If copy protection is used during DVD-Video playback, the resolution on the EM8550 analog YPbPr/RGB outputs may not be higher than standard definition (720x480 or 720x576). If the output is configured to be progressive YPbPr, only 480p video may be generated.

Configurable chroma filters

The four available chrominance low pass filters are shown in Table 6, page 48. The 1.3 MHz low pass filter is recommended when the composite and s-video outputs are used. Filter performance is dependent on the NTSC/PAL decoder used in the display. If only the YPbPr output is used, the 2.0 MHz low pass filter should be selected for maximum color detail. For RGB output mode, the chrominance filters can be disabled, enabling full-bandwidth color information to be present.

Table 6. Recommended(1) chroma filter applications.

Cutoff (MHz)	Recommended application
0.65	NTSC, PAL
1.0	NTSC, PAL
1.3	NTSC, PAL
2.0	YPbPr

1. Filters may be selected for custom applications, e.g., the 1.3MHz filter may be selected for composite PAL.

Luminance filters

EM8550 uses a single low pass filter and a single extended mode filter for both PAL and NTSC. Disabling the filter results in increased sharpness at the expense of aliasing. The efficiency of the filter is dependent on the television used. Either of these

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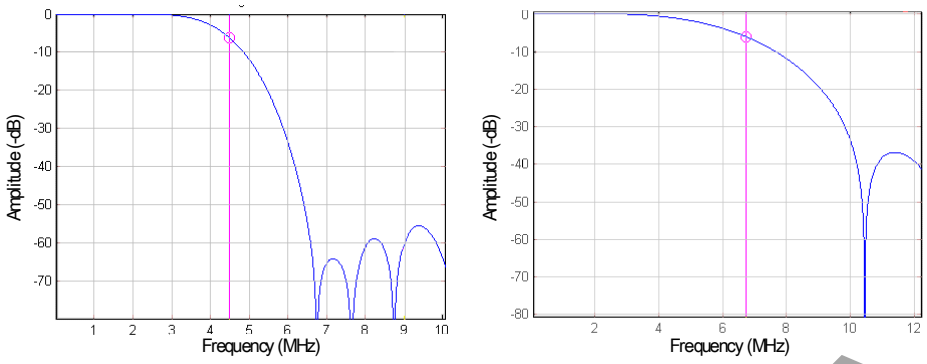
filters can be combined with optional notch filtering (NTSC only). It may be used to prevent cross-color (artificial colors appearing in regions of very fine detail), but this reduces image sharpness.



Double all frequencies shown (expand the scale of the frequency axis) for 480p.
These filters are selected via bits [9] and [7] of the CONFIG2 register.

Figure 40. Available low pass filters for NTSC and PAL.

VBI data support

The TV encoder supports closed captioning (CC), extended data services (XDS) and wide screen signalling (WSS) functions. CC carries sub-titling and captioning information. XDS sends supplementary information (described in EIA-608) that includes items such as the type of program being viewed, the program rating, and the time of day. WSS transmits the aspect ratio of the program being viewed to the TV; it also carries copy generation management system (CGMS-A) information.

Closed captioning data is transmitted on line 21/22 (i.e., 21 for 525/60 and 22 for 625/50). It can also use line 284/335 if XDS is not used. Bits [5:4] of the CONFIG register control the use of lines 21/22 and 284/335. Two data bytes are transmitted for each field. In most implementations, an interrupt service routine (ISR) or similar mechanism writes CC_DATA during VSYNC. EIA-608 describes the actual meaning and format of the transmitted data. XDS uses line 284 to transmit rating and content information; it is otherwise similar to CC.

CGMS-A and WSS data is present on the composite output, the Y signal of the S-Video output, and the Y signal of YPbPr output in 480i mode. WSS, which includes CGMS-A signalling, is present on line 23 for 625/50 systems (ITU-R BT.1119), and on lines 20 and 283 for 525/60 systems (IEC 61880). In both cases, 14 bits of data are transmitted. CRC is automatically generated for 525/60 systems (it is not needed for 625/50 systems).

Pedestal control (NTSC)

Use bit [15] of CONFIG2 to turn pedestal on (‘0’ for USA) or off (‘1’ is Japan). When pedestal is off, the video gain is adjusted to maintain the proper white level.

Timing diagrams

The timing diagrams below show video timing when outputting NTSC signals.

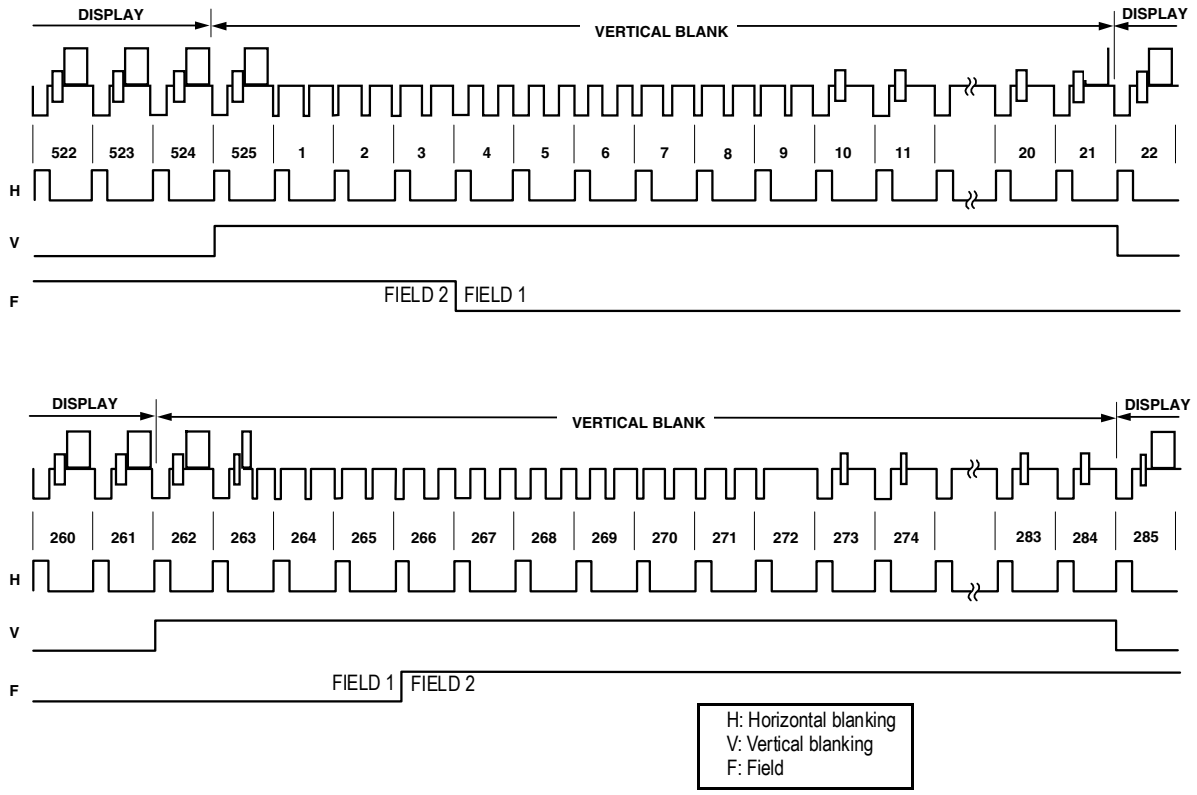


Figure 41. NTSC mode.

The timing diagrams below show video timing when outputting PAL signals.

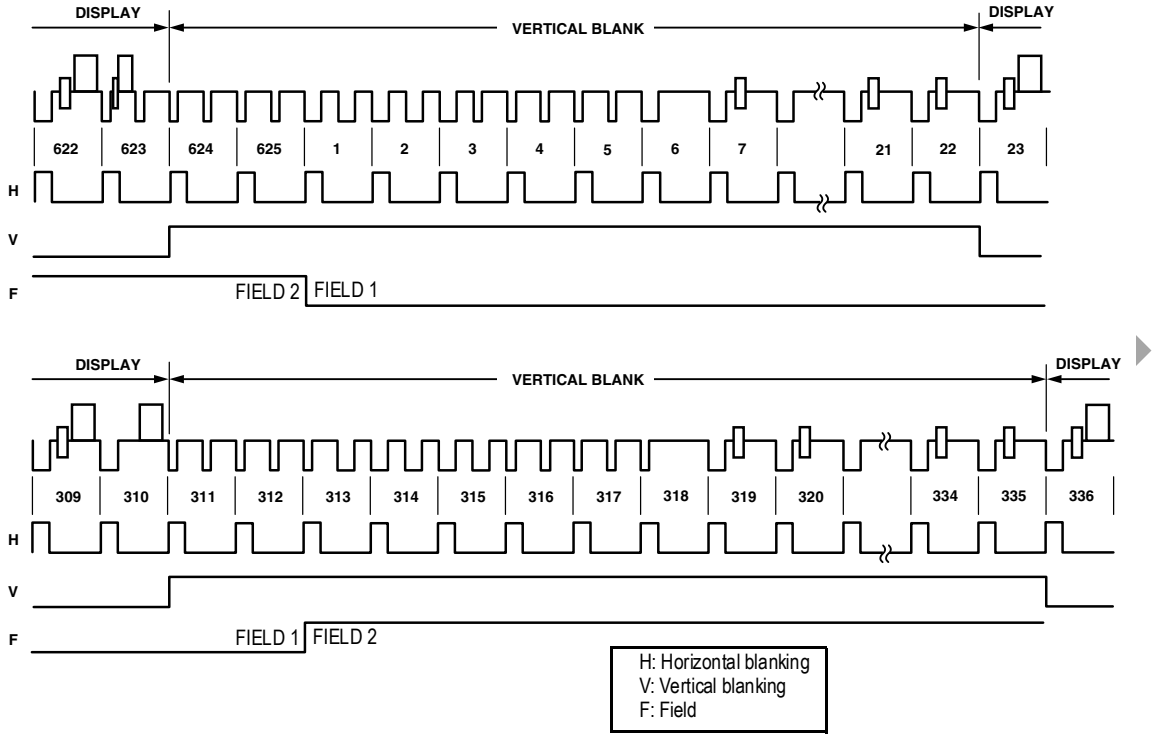


Figure 42. PAL mode.

Video Input Interface

The EM8550 video input interface receives digital video data (from an external video decoder) for display as the main television program. VBI data on this input is ignored. Since there is no blanking signal input, the active video region to capture is determined by internal registers.

The video input port is designed to capture video data from an HDTV decoder chip, a NTSC/PAL video decoder chip, or from an IEEE 1394 to CCIR656 interface chip in either 8-/16-bit CCIR601 or 8-/16-bit CCIR656 YCbCr video data formats. The input port must operate in slave mode, synchronized to the input clock and sync signals. The input port is designed to support video rates up to 80 MHz (160 MBps) and resolutions up to 720p or 1080i.The video input port's two write channels to the EM8550 SDRAM are used for luma and chroma data. The input port has two options for reducing the video data: downsampling the chroma from 4:2:2 to 4:2:0 and using a lossy packing algorithm.

After processing, the video is stored in SDRAM in 4:2:2 or 4:2:0 YCbCr format, with an active resolution of 720×480 or 720×576. This input may be converted to progressive using either field merging or scan line interpolation.

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CCIR601 timing diagrams

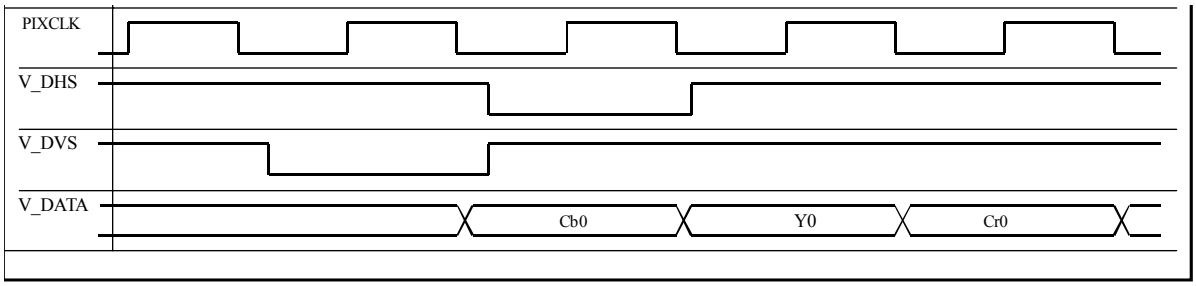

Figure 43. CCIR601 video input timing diagram: even field.

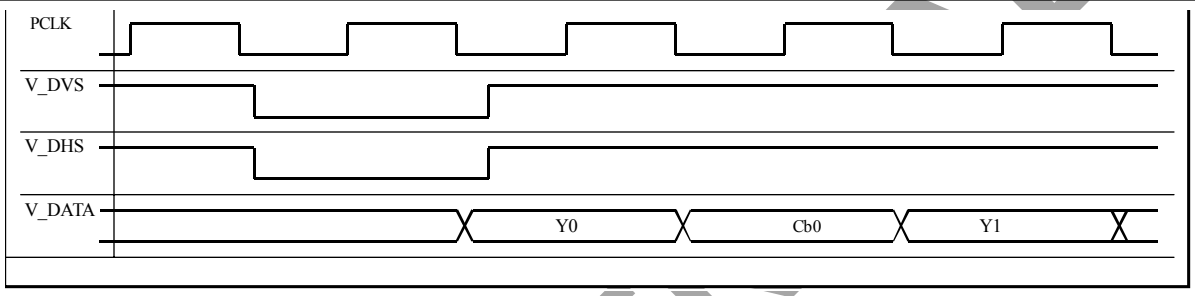

Figure 44. CCIR601 video input timing diagram: odd field.

If V_DHS is active at the active edge of V_DVS, the next field is odd; otherwise it is even.

CCIR656 timing

Four byte sequences, SAVs (Start of Active Video) and EAVs (End of Active Video), are embedded in the video data. They delimit active video and provide information on the incoming video field.

The EM8550 also supports VIP 2.0.

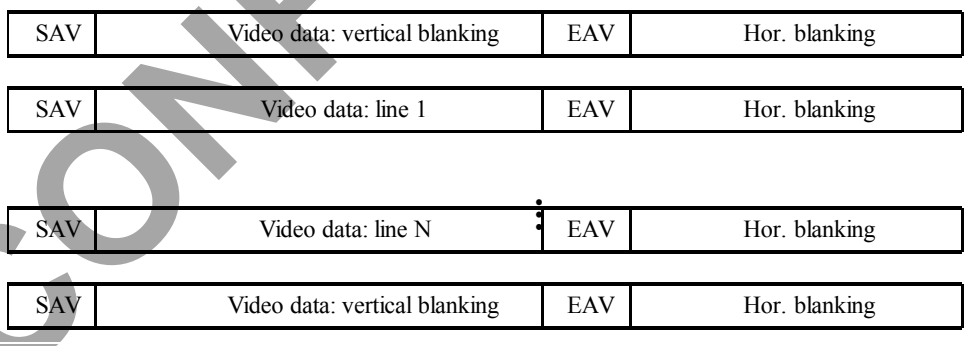

Figure 45. CCIR656 video input timing diagram.

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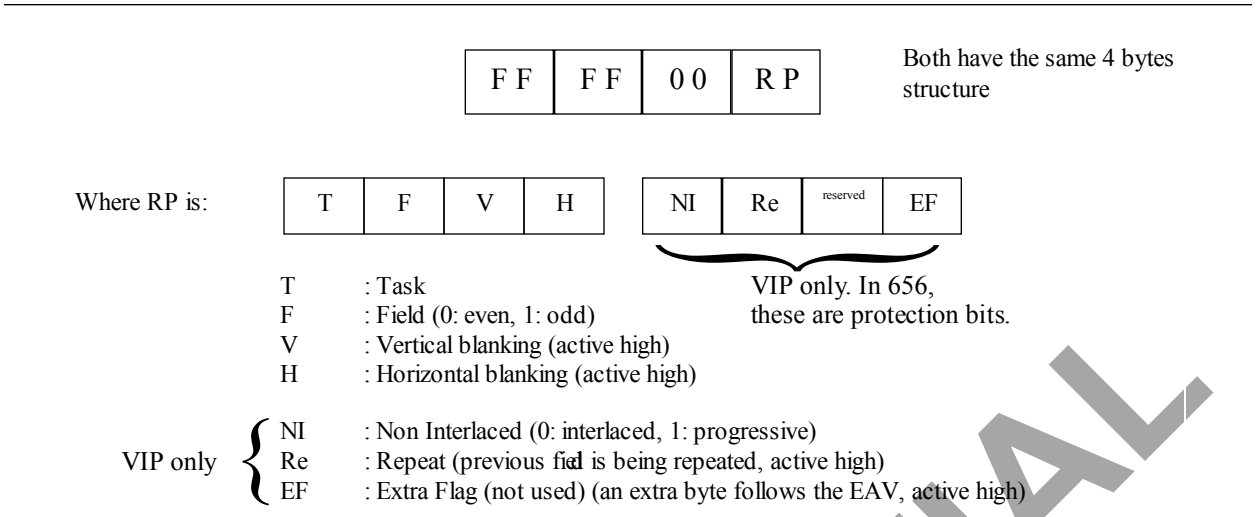

Figure 46. SAV and EAV sequences.

This protocol also allows the transfer of ancillary data within the horizontal blankings, but it is not extracted.

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Audio

The audio engine interfaces with external devices such as an amplifier, speaker, or a microphone for Karaoke support. EM8550 supports 6-channel PCM outputs or an AC3 output.

The audio engine consists of four main modules: audio synchronization, AC3_MPEG, PCM, and the serial output block. The audio decoder block supports the following audio bitstream formats:

- Dolby Digital (AC-3)
- ISO11172-3 MPEG layers 1, 2, and 3
- Linear PCM non-compressed data from DVD-Audio or DVD-Video
- DTS Digital Out over S/PDIF

The audio output is compressed or uncompressed 16/20/24 bit 32/44.1/48/88.2/96kHz data output serially via an I^2S or S/PDIF (IEC958) interface.

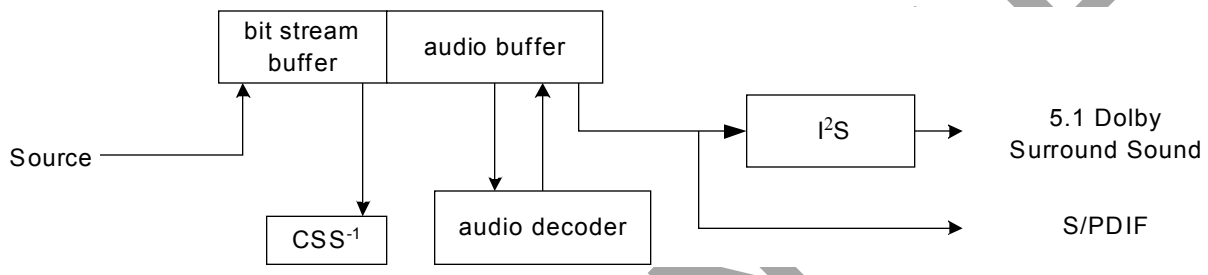

Figure 47. Audio pipeline diagram.

Audio Decoder

Audio sync. block

The sync block receives the bitstream data from the DRAM controller through a standard 8 bit port (data-valid-ready) and routes the data to either the AC3_MPEG block or the DVD_PCM block, depending on the type of bitstream being processed. Only one of the two blocks is active at a given time, and a complete reset of the audio block is required in order to switch from one to the other. The sync block contains some hardware counters to assist the RISC with audio/video synchronization. See "Audio Synchronization" on page 55. for more details.

AC3_MPEG

The AC3_MPEG core is an hard-coded logic block consisting of a ROM coefficient table, 1Kx16 local SRAM and decoding logic which is designed to decode Dolby Digital (AC3) and MPEG bitstreams. The AC3_MPEG core accepts an 8-bit wide input stream directly from an external DRAM and will output 16/20 bit compressed or non-compressed stereo linear PCM data. The operation of the audio decoder core requires an exact sequence of initialization and programming steps, as presented in the EM8550 Software API manual.

PCM DVD-Audio module

The PCM DVD-Audio module is a sub-block designed to convert linear PCM data in DVD-Audio format to 2-channel stereo output for the serial output block. The PCM audio block receives 1-6 channels of 44.1kHz, 48kHz, 88.2kHz, and 96kHz sampled audio which is quantized in 16-bit Linear PCM data directly from DRAM. The PCM block outputs linear PCM audio that is down mixed and downsampled by 1, 2, or 4 based upon the input and output sample rates. The PCM block contains two main blocks, a down mix block followed by a downsample block.

Serial output/gain control

The serial output interface receives an audio bitstream from either the AC3_MPEG block or PCM DVD Audio/Video module and it converts these data into a serial stream compatible with the I^2S or S/PDIF=IEC958 specifications. The master serial clock (x256 or x384) comes from an external source.

Audio Synchronization

The audio synchronization block enables the DRAM input port to interface with either the AC3_MPEG block or the PCM block and to assist the RISC with audio synchronization. Audio synchronization is primarily handled by the RISC, and the process is identical for AC3, MPEG or PCM audio formats. The audio engine receives an audio bitstream (from EM8550 DRAM, through the DRAM controller). After a reset, or flush, the AUDIO_Bytecount register is initialized by the RISC (most likely to 0), and is automatically incremented for each byte transferred from DRAM.

Audio Output

The EM8550 provides full 5.1 channel output to an external 6-channel DAC. Audio can also be downmixed to 2-channel stereo output. Digital audio outputs can be delivered via S/PDIF and I^2S simultaneously for PCM only. For compressed AC-3 and DTS, I^2S is inactive. The serial interface is part of the EM8550 audio block. It receives data/samples from the audio decoder core or the PCM block, scales them for gain control, serializes them and sends them simultaneously to a I^2S and a S/PDIF serial output.

Gain control block

The gain control block requests samples/data from either the audio decoder core (on DIN0) or the PCM block (on DIN1) by toggling the LRCLKIN signal. A rising edge of LRCLKIN requests a left sample, and a falling edge requests a right sample. The selected block indicates a valid sample by setting the corresponding VLDIN signal high.

The input samples are scaled and clipped (if G bit=1) or left unchanged (if G bit is 0)

The result is truncated to 16/18/20 bits or left unchanged, depending on the trunc bits, and sent out to the shift register block on SR_DATA.

When the input sample is not valid, the output sample is also flagged as not valid (SR_VLD = 0) and SR_DATA is forced to 0.

Shift register block

The serial block takes 24-bit audio data from the gain control block and outputs the audio data in S/PDIF and serial output modes. The serial control register 0 selects the alignment of the data and polarity of all of the output signals.

I^2S output

The I^2S interface operates in 32-bit mode (sframeout = sclkout/64) except when then align field is equal to 31, in which case it operates in 16-bit mode (sframeout = sclkout/32).

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Electrical Specifications

The following test conditions apply unless otherwise specified:

- $V_{DD\ PLL}$ = 1.8V
- $V_{DD\ VIDEO\ DAC}$ = 3.3V
- RSET = 82 Ω (double termination) or 200 Ω (single termination)
- TA = 0-70°C

Absolute maximum ratings(1)

3.3V supply voltage (V_{DD33} to V_{SS}) . . . . . 3.3V ± 10%

1.8V supply voltage (V_{DD} to V_{SS}) . . . . . 1.8V ± 5%

Voltage on any pin . . . . . V_{SS} - 0.7V to 5.5V

ESD classification. . . . . Class 1

Operating temperature range

. . . . . 0° C to 70° C

501 BGA thermal information

Thermal resistance, θ_{JA} (typical). . . . . 27° C/W

Maximum power dissipation . . . . . .(typical) 1.3W

Maximum storage temperature range . . . . . -65° C to 150° C

Maximum junction temperatures . . . . . .120° C

Maximum lead temperature (soldering 10s). . . . . 300° C

Table 7. 1.8V power supply.

Parameter	Symbol	Test condition	Min	Typ	Max	Units
Operating voltage	V_{DD18} $PLLV_{DD18}$		1.7	1.8	1.9	V
Power supply current	I_{DD}	CLK = 27.0 MHz, V_{DD18} = AV_{DD18} = $PLLV_{DD18}$ = 1.8V, outputs not loaded Playback (normal operation)	-	300	-	mA

Note 1. CAUTION: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
IMPORTANT: All power supply pins must be powered up and powered down simultaneously to avoid latch-up.

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The EM8550 has two sets of connections to a 3.3V (nominal) power source. The VDD_IO pins power the device I/O buffers, while the AVDD pins power the internal video DACs. The current consumed from the AVDD pins varies depending on whether single termination (75 ohm) or double termination (37.5 ohm effective) is employed on the analog video outputs.

Table 8. 3.3V power supply.

Parameter	Symbol	Test condition	Min	Typ	Max	Units
Operating voltage	V_{DDIO} AV_{DD}		2.97	3.3	3.63	V
Power supply current	I_{VDDIO}	CLK = 27.0 MHz, V_{VDDIO} = 3.3V Playback (normal operation)	-	100	-	mA
Power supply current	I_{AVDD}	CLK = 27.0 MHz, V_{VDDIO} = 3.3V DACs enabled, single termination	-	90	-	mA
Power supply current	I_{AVDD}	CLK = 27.0 MHz, V_{VDDIO} = 3.3V DACs enabled, double termination	-	170	-	mA
Power supply current	I_{AVDD}	CLK = 27.0 MHz, V_{VDDIO} = 3.3V DACs disabled	-	0	-	mA

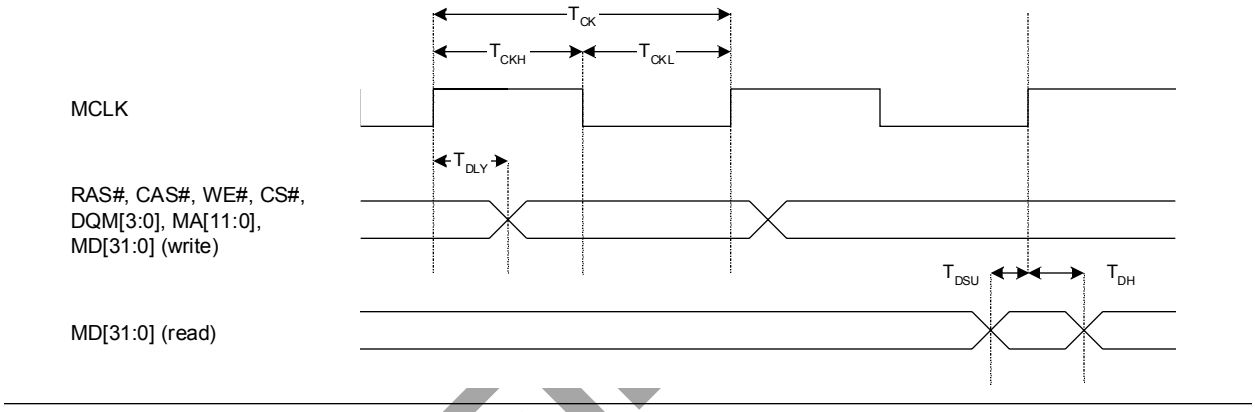

Figure 48. MPEG SDRAM interface timing diagram.

Table 9. MPEG SDRAM interface (electrical specifications).

Parameter	Symbol	Test condition	Min	Typ	Max	Units
DC Characteristics						
Input logic high voltage	V_{IH}	V_{DD33} = 3.63V	2.0	-	5.75	V
Input logic low voltage	V_{IL}	V_{DD33} = 2.97V	0	-	0.8	V
Output logic high voltage	V_{OH}	I_{OH} = -8 mA, V_{DD33} = 3.63V	2.4	-	-	V
Output logic low voltage	V_{OL}	I_{OL} = 8 mA, V_{DD33} = 2.97V	-	-	0.4	V
Input leakage current	I_{IH}, I_{IL}	V_{DD33} = 3.63V, input = 0V to 3.3V	-	-	± 10	µA
Input/output capacitance	C_{IN}, C_{OUT}	f = 1 MHz, T_A = 25°C Notes (1), (2)	-	8	-	pF
Three-state output current leakage	I_{OZ}		-	-	10	µA
AC Characteristics						
MCLK frequency	F_{MCLK}		-	-	125	MHz
MCLK period	T_{CK}		8.0	-	-	ns
MCLK high time	T_{CKH}		3.0	-	-	ns

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Table 9. MPEG SDRAM interface (electrical specifications).

Parameter	Symbol	Test condition	Min	Typ	Max	Units
MCLK low time	T_{CKL}		3.0	-	-	ns
Memory controller outputs valid delay from MCLK rising	T_{DLY}	Notes(3)	2.5	-	6.8	ns
MD [31:0] setup to MCLK rising (read)	T_{DSU}		2.0	-	-	ns
MD [31:0] hold from MCLK rising (read)	T_{DH}		1.5	-	-	ns
Memory controller outputs rise time	T_R	Notes(4)	-	-	3.0	ns
Memory controller outputs fall time	T_F	Notes(5)	-	-	3.0	ns

1. Test performed with CL = 40 pF, IOL = 4 mA, IOH = -4 mA. Input reference level is 1.5V for all inputs. V_{IH} = 3.0V, V_{IL} = 0V.
2. Guaranteed by characterization.
3. Parameter applies to MA [11:0], DQM [3:0], RAS#, CAS#, WE#, CS#, and to MD [31:0] on SDRAM writes.
4. Measured from V_{OUT} = 0.8V to V_{OUT} = 2.0V. C_L = 12pf
5. Measured from V_{OUT} = 2.0V to V_{OUT} = 0.8V. C_L = 12pf

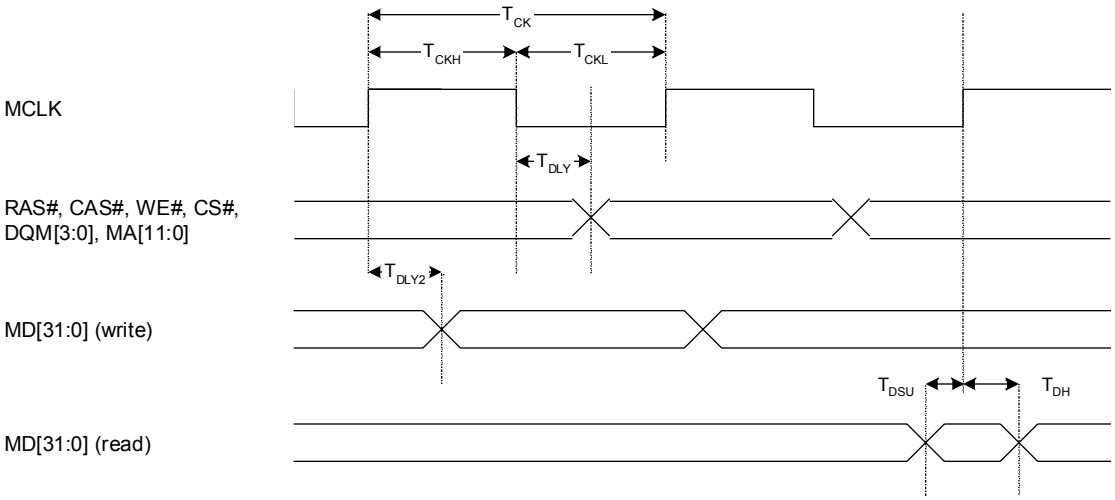

Figure 49. MAC interface timing diagram.

Table 10. MAC interface -- RISC SDRAM and Flash memory (electrical specifications).

Parameter	Symbol	Test condition	Min	Typ	Max	Units
DC Characteristics						
Input logic high voltage	V_{IH}	V_{DD33} = 3.63V	2.0	-	5.75	V
Input logic low voltage	V_{IL}	V_{DD33} = 2.97V	0	-	0.8	V
Output logic high voltage	V_{OH}	I_{OH} = -8 mA, V_{DD33} = 3.63V	2.4	-	-	V
Output logic low voltage	V_{OL}	I_{OL} = 8 mA, V_{DD33} = 2.97V	-	-	0.4	V
Input leakage current	I_{IH}, I_{IL}	V_{DD33} = 3.63V, input = 0V to 3.3V	-	-	± 10	µA
Input/output capacitance	C_{IN}, C_{OUT}	f = 1 MHz, T_A = 25°C Notes (1), (2)	-	8	-	pF
Three-state output current leakage	I_{OZ}		-	-	10	µA
AC Characteristics						
MCLK frequency	F_{MCLK}		-	-	83.3	MHz

Table 10. MAC interface -- RISC SDRAM and Flash memory (electrical specifications).

Parameter	Symbol	Test condition	Min	Typ	Max	Units
MCLK period	T_{CK}		12.0	-	-	ns
MCLK high time	T_{CKH}		4.8	-	-	ns
MCLK low time	T_{CKL}		4.8	-	-	ns
Memory controller outputs valid delay from MCLK falling	T_{DLY}	Note (3)	0	-	2.5	ns
Memory data output valid delay from MCLK rising	T_{DLY2}	Note (4)	3	-	?	ns
MD [31:0] setup to MCLK rising (read)	T_{DSU}		5.0	-	-	ns
MD [31:0] hold from MCLK rising (read)	T_{DH}		2.0	-	-	ns
Memory controller outputs rise time	T_R	Note (5)	-	-	3.0	ns
Memory controller outputs fall time	T_F	Note (6)	-	-	3.0	ns

1. Test performed with CL = 40 pF, IOL = 4 mA, IOH = -4 mA. Input reference level is 1.5V for all inputs. V_{IH} = 3.0V, V_{IL} = 0V.
2. Guaranteed by characterization.
3. Parameter applies to MA [11:0], DQM [3:0], RAS#, CAS#, WE#, CS#.
4. Parameter applies to MD [31:0] on SDRAM writes.
5. Measured from V_{OUT} = 0.8V to V_{OUT} = 2.0V. C_L = 12pf
6. Measured from V_{OUT} = 2.0V to V_{OUT} = 0.8V. C_L = 12pf

Table 11. Analog RGB/YPbPr video output (electrical specifications).

Parameter	Symbol	Test condition	Min	Typ	Max	Units
DC Characteristics						
DAC resolution		Note (1)	-	10	-	Bits
Full-scale output current	VID_{IOUT}	AV_{DD33} = 3.3V	33	35	37	mA
White level relative to blanking						
0 IRE blanking pedestal			16.8	18.7	20.6	mA
7.5 IRE blanking pedestal			15.3	17	18.7	mA
Black level relative to blanking						
0 IRE blanking pedestal			0	0	0	mA
7.5 IRE blanking pedestal			1.8	2	2.2	mA
Sync amplitude (bi-level)						
0 IRE blanking pedestal			7.2	8	8.8	mA
7.5 IRE blanking pedestal			6.8	7.6	8.3	mA
Sync amplitude (tri-level)						
High pulse			3.6	4	4.4	mA
Low pulse			3.6	4	4.4	mA
Total			7.2	8	8.8	mA
Output impedance			-	12	-	kΩ
Output capacitance	VID_{COUT}	f = 1 MHz, VID_{OUT} = 0 mA, T_A = 25°C, Note (1)	-	15	-	pF
Output compliance range		T_A = 25°C, Note (2)	-	1.4	-	V
Integral nonlinearity	VID_{INL}		-	0.5	± 2	LSB
Differential nonlinearity	VID_{DNL}		-	0.5	± 1	LSB
Level error			-	-	± 10	%
DAC-to-DAC matching			-	-	± 5	%
AC Characteristics						

Table 11. Analog RGB/YPbPr video output (electrical specifications).

Parameter	Symbol	Test condition	Min	Typ	Max	Units
Blank rise/fall time		Note (1)				
480i, 576i			120	140	160	ns
480p, 576p			60	70	80	ns
720p, 1080i			34	54	74	ns
Sync rise/fall time						
480i, 576i			120	140	160	ns
480p, 576p			60	70	80	ns
720p, 1080i			34	54	74	ns
Output skew		Note (2)	-	5	-	ns
DAC-to-DAC crosstalk		Note (2)	-	-36	-	dB
Glitch energy		Using analog output filter. Includes clock and data feedthrough. Note (2)	-	75	-	pV-s
Power supply rejection ratio	PSRR	Note (2)	-	0.1	0.5	%/%

1. Guaranteed by characterization.
2. Guaranteed by design.

Table 12. Analog composite and S-Video video outputs (electrical specifications).

Parameter	Symbol	Test condition	Min	Typ	Max	Units
DC Characteristics						
DAC resolution		Note (1)	-	10	-	Bits
Full-scale output current	VID_{IOUT}	AV_{DD33} = 3.3V	33	35	37	mA
White level relative to blanking						
0 IRE blanking pedestal			16.8	18.7	20.6	mA
7.5 IRE blanking pedestal			15.3	17	18.7	mA
Black level relative to blanking						
0 IRE blanking pedestal			0	0	0	mA
7.5 IRE blanking pedestal			1.8	2	2.2	mA
Sync amplitude						
0 IRE blanking pedestal			7.2	8	8.8	mA
7.5 IRE blanking pedestal			6.8	7.6	8.3	mA
Burst amplitude (peak)						
(M) NTSC			6.8	7.6	8.3	mA
(B, D, G, H, I) PAL			7.2	8.0	8.8	mA
(M) PAL			7.2	8.0	8.8	mA
Output impedance			-	12	-	kΩ
Output capacitance	VID_{COUT}	f = 1 MHz, VID_{OUT} = 0 mA, T_A = 25°C, Note (2)	-	15	-	pF
Output compliance range		T_A = 25°C, Note (2)	-	1.4	-	V
Integral nonlinearity	VID_{INL}		-	0.5	± 2	LSB
Differential nonlinearity	VID_{DNL}		-	0.5	± 1	LSB
Level error			-	-	± 10	%
DAC-to-DAC matching			-	-	± 5	%
AC Characteristics						

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Table 12. Analog composite and S-Video video outputs (electrical specifications).

Parameter	Symbol	Test condition	Min	Typ	Max	Units
Burst envelope rise/fall time		Note (2)	200	300	400	ns
Blank rise/fall time (M) NTSC (B, D, G, H, I) PAL (M) PAL			 120 200 200	 140 300 300	 160 400 400	 ns ns ns
Sync rise/fall time (M) NTSC (B, D, G, H, I) PAL (M) PAL			 120 200 200	 140 250 250	 160 300 300	 ns ns ns
Differntial phase			-	4	-	degrees
Differntial gain			-	4	-	%
Luminance nonlinearity			-	2	-	%
Hue accuracy			-	3	-	degrees
Color saturation accuracy			-	3	-	%
Residual subcarrier			-	0.5	-	IRE
SNR (per EIA-250-C)			-	48	-	dB
SCH phase			- 40	0	+ 40	degrees
Output skew			-	5	-	ns
DAC-to-DAC crosstalk			-	-36	-	dB
Glitch energy		Using analog output filter. Includes clock and data feedthrough.	-	75	-	pV-s
Power supply rejection ratio	PSRR	Note (1)	-	0.1	0.5	%/%

1. Guaranteed by design.
2. Guaranteed by characterization.

Table 13. I^2S input and output interfaces (electrical specifications)

Parameter	Symbol	Test condition	Min	Typ	Max	Units
DC Characteristics						
Input logic high voltage	V_{IH}	V_{DD33} = 3.63V	2.0	-	5.75	V
Input logic low voltage	V_{IL}	V_{DD33} = 2.97V	0	-	0.8	V
Output logic high voltage	V_{OH}	I_{OH} = -1 mA, V_{DD33} = 3.63V	2.4	-	-	V
Output logic low voltage	V_{OL}	I_{OL} = 3 mA, V_{DD33} = 2.97V	0	-	0.4	V
Input leakage current	I_{IH}, I_{IL}	V_{DD33} = 3.63V, input = 0V to 3.3V	-	-	± 10	µA
Input/output capacitance	C_{IN}, C_{OUT}	SCOUT = 1.024 MHz, T_A = 25°C, Notes (1), (2)	-	-	10	pF
AC Characteristics						
ACLK, SCOUT frequency			-	1.024	-	MHz
ACLK, SCOUT pulse width high	t_{PWH}	T = 1/frequency	0.35T	-	-	ns
ACLK, SCOUT pulse width low	t_{PWL}		0.35T	-	-	ns
ACLK, SCOUT rise/fall time	t_R, t_F	T = 1/frequency, Notes (1), (2)	0.15T	-	-	ns
SDOUT, SFOUT output delay time	$t_{DLY:DATA}$	T = 1/frequency	-	-	0.8T	ns
SDOUT, SFOUT output hold time	$t_{HD:DATA}$		0	-	-	ns
SDIN input hold time	$t_{HD:DATA}$		0	-	-	ns
SDIN input setup time	$t_{SU:DATA}$		0.2T	-	-	ns

1. Test performed with CL = 40 pF, I_{OL} = 4 mA, I_{OH} = -4 mA. Input reference level is 1.5V for all inputs. V_{IH} = 3.0V, V_{IL} = 0V.
2. Guaranteed by characterization.

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Table 14. S/PDIF output interface (electrical specifications).

Parameter	Symbol	Test condition	Min	Typ	Max	Units
DC Characteristics						
Output logic high voltage	V_{OH}	I_{OH} = -1 mA, V_{DD33} = 3.63V	2.4	-	-	V
Output logic low voltage	V_{OL}	I_{OL} = 3 mA, V_{DD33} = 2.97V	0	-	0.4	V
Output capacitance	C_{IN}, C_{OUT}	SD_IN = SD_OUT = 1.024 MHz, T_A = 25°C, Notes (1), (2)	-	-	10	pF
AC Characteristics						
S/PDIF OUT frequency			-	1.024	-	MHz
S/PDIF OUT rise/fall time	t_R, t_F	T = 1/frequency, Notes (1), (2)	0.15T	-	-	ns

1. Test performed with CL = 40 pF, IOL = 4 mA, IOH = -4 mA. Input reference level is 1.5V for all inputs. VIH = 3.0V, VIL = 0V.
2. Guaranteed by characterization.

Table 15. GCLK input (electrical specifications).

Parameter	Symbol	Test condition	Min	Typ	Max	Units
DC Characteristics						
Input logic high voltage	V_{IH}	V_{DD33} = 3.63V	2.0	-	5.75	V
Input logic low voltage	V_{IL}	V_{DD33} = 2.97V	0	-	0.8	V
Input leakage current	I_{IH}, I_{IL}	V_{DD33} = 3.63V, input = 0V to 3.3V	-	-	± 10	µA
Input capacitance	CIN, COUT	f = 1 MHz, T_A = 25°C Notes (1), (2)	-	8	-	pF
AC Characteristics						
GCLK frequency			-	27	-	MHz
GCLK pulse width high	t_{PWH}		15	-	-	ns
GCLK pulse width low	t_{PWL}		15	-	-	ns
Rise/fall time	t_r, t_f	Notes (1), (2)	-	-	3	ns

1. Test performed with CL = 40 pF, I_{OL} = 4 mA, I_{OH} = -4 mA. Input reference level is 1.5V for all inputs. V_{IH} = 3.0V, V_{IL} = 0V.
2. Guaranteed by characterization.

Table 16. GPIO pins (electrical specifications).

Parameter	Symbol	Test condition	Min	Typ	Max	Units
Input logic high voltage	V_{IH}	V_{DD33} = 3.63V	2.0	-	5.75	V
Input logic low voltage	V_{IL}	V_{DD33} = 2.97V	0	-	0.8	V
Output logic high voltage	V_{OH}	I_{OH} = -8 mA, V_{DD33} = 3.6V	3.0	-	-	V
Output logic low voltage	V_{OL}	I_{OL} = 8 mA, V_{DD33} = 2.97V	-	-	0.4	V
Input leakage current	I_{IH}, I_{IL}	V_{DD33} = 3.63V, input = 0V to 3.3V	-	-	± 10	µA
Input/output capacitance	C_{IN}, C_{OUT}	f = 1 MHz, T_A = 25°C Notes (1), (2)	-	8	-	pF

1. Test performed with CL = 40 pF, I_{OL} = 4 mA, I_{OH} = -4 mA. Input reference level is 1.5V for all inputs. V_{IH} = 3.0V, V_{IL} = 0V.
2. Guaranteed by characterization.

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Comprehensive Pin Listing

Table 17. Comprehensive descriptive pin listing.

Pin	Pin Name	Description	I/O	Alternate	Power Strapping
G2	DAC1_SCOUT	DAC1 L channel negative terminal	O	-	-
G1	DAC1_ACLK_256	DAC1 L channel positive terminal	O	-	-
H2	DAC1_SFOUT	DAC1 R channel negative terminal	O	-	-
H1	DAC1_SDOUT	DAC1 R channel positive terminal	O	-	-
G3	DAC2_SCOUT	DAC2 L channel negative terminal	O	-	-
H3	DAC2_ACLK_256	DAC2 L channel positive terminal	O	-	-
K3	DAC2_SFOUT	DAC2 R channel negative terminal	O	-	-
J3	DAC2_SDOUT	DAC2 R channel positive terminal	O	-	-
J2	DAC3_SCOUT	DAC3 L channel negative terminal	O	-	-
J1	DAC3_ACLK_256	DAC3 L channel positive terminal	O	-	-
K2	DAC3_SFOUT	DAC3 R channel negative terminal	O	-	-
K1	DAC3_SDOUT	DAC3 R channel positive terminal	O	-	-
L3	AUD_SPDIFOUT	SPDIF digital out	I	-	-
A4	AVDD_VDAC	VDD3_3 DAC	I	-	-
D23	AVDD_SPLL	System PLL Power	-	-	-
D24	AVDD_VPLL	Video PLL Power	-	-	-
A2	AVDD_CVBS	VDD3_3 CVBS	I	-	-
C2	AVDD_U	VDD3_3_U	I	-	-
D2	AVDD_V	VDD3_3 V	I	-	-
B2	AVDD_Y	VDD3_3 Y	I	-	-
B4	AVSS_VDAC	VSS_DAC	I	-	-
D22	AVSS_SPLL	System PLL Ground	-	-	-
E24	AVSS_VPLL	Video PLL Ground	-	-	-
A13	BREAKPT	DEBUG IF: Breakpoint	I	-	-
M25	SM_CAS#	System Memory SDRAM Column addr. Strobe	O	-	-
AG18	RTC_CLKIN	Not used.	-	-	-
A24	CLKOUT	27 MHz internal Oscillator output (buffered)	O	-	-
AA25	IDE_CS0#	IDE Chip Select 0	O	-	-
AB26	IDE_CS1#	IDE Chip Select 1	I/O	DVD loader Data Error	-
D19	UART0_CTS#	UART0: Clear to Send	I	-	-
AF18	UART1_CTS#	UART1: Clear to Send	I	-	-
A1	CVBS	Analog Video output CVBS	O	-	-
A3	AVSS_CVBS	VSS CVBS	-	-	-
F3	DABCK	Bitclk	O		-
F4	AUD_CH1_VDD	DAC1 VCC 3V3	-	-	-
G4	AUD_CH2_VSS	DAC1 VSS	-	-	-
H4	AUD_CH3_VDD	DAC2 VCC 3V3	-	-	-
J4	AUD_CH4_VSS	DAC2 VSS	-	-	-
K4	AUD_CH5_VDD	DAC3 VCC 3V3	-	-	-
L4	AUD_CH6_VSS	DAC3 VSS	-	-	-
AD27	IDE_ACK#	IDE DMA acknowledge	O	DVD host SCLK	-
M4	DADAT	Serial data output	O		-

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Table 17. Comprehensive descriptive pin listing.

Pin	Pin Name	Description	I/O	Alternate	Power Strapping
M3	DALRK	Serial data L/R clk	O		-
F2	DAMCK	Serial audio clk out	I/O		-
A14	DBGACK	DEBUG IF: Debug Acknowledge	O	-	-
A15	DBGRQ	DEBUG IF: Debug Request	I	-	-
C19	UART0_DCD#	UART0: Data Carrier Detect	I	-	-
AE18	UART1_DCD#	UART1: Data Carrier Detect	I	-	-
AB27	DVD_CLKIN	-	I	DVD Loader Clock	-
AB24	IDE_DMAREQ	IDE DMA request	I	DVD host RXD	-
F26	SM_DQM[0]	System Memory SDRAM I/O mask 0	O	-	-
M24	SM_DQM[1]	System Memory SDRAM I/O mask 1	O	-	-
R25	SM_DQM[2]	System Memory SDRAM I/O mask 2	O	-	-
L25	SM_DQM[3]	System Memory SDRAM I/O mask 3	O	-	-
B19	UART0_DSR#	UART0: Data Set Ready	I	-	-
AD18	UART1_DSR#	UART1: Data Set Ready	I	-	-
B18	UART0_DTR#	UART0: Data Terminal Ready	O	-	-
AE19	UART1_DTR#	UART1: Data Terminal Ready	O	-	-
AF21	VFD_CLKOUT	VFD: Clock out to CTRL	O	-	-
AE20	VFD_DIN	VFD: Data from VFD CTRL	I	-	-
AG21	VFD_DOUT	VFD: Data to VFD Ctrl	O	-	-
Y24	FLASH_CFG[0]	Flash configuration (16# / 32 bits flash width)	I	-	-
AA27	FLASH_CFG[1]	Flash configuration (1# / 2 Chip select signals)	I	-	-
Y26	FLASH_CS[0]#	Flash Chip Select 0	O	-	-
Y27	FLASH_WE#	Flash Write Enable	O	-	-
AD20	VFD_STB	VFD: Strobe output	O	-	-
AG9	NC	No Connection	O	-	-
AF9	NC	No Connection	O	-	-
AE9	NC	No Connection	O	-	-
AD9	NC	No Connection	O	-	-
AG8	NC	No Connection	O	-	-
AF8	AS_ALE	Local Peripheral Bus Address Strobe	O	-	-
AE8	NC	No Connection	O	-	-
AD8	NC	No Connection	O	-	-
AG7	NC	No Connection	O	-	-
AG15	NC	No Connection	O	-	-
AG13	LPB_HSEL#	Local Peripheral Bus Device Chip Select	O	-	-
AD14	LPB_AD[0]	Local Peripheral Bus Address/Data Bit 0	I/O	-	-
AF13	LPB_AD[1]	Local Peripheral Bus Address/Data Bit 1	I/O	-	-
AE11	LPB_AD[10]	Local Peripheral Bus Address/Data Bit 10	I/O	-	-
AD11	LPB_AD[11]	Local Peripheral Bus Address/Data Bit 11	I/O	-	-
AG10	LPB_AD[12]	Local Peripheral Bus Address/Data Bit 12	I/O	-	-
AF10	LPB_AD[13]	Local Peripheral Bus Address/Data Bit 13	I/O	-	-
AE10	LPB_AD[14]	Local Peripheral Bus Address/Data Bit 14	I/O	-	-
AD10	LPB_AD[15]	Local Peripheral Bus Address/Data Bit 15	I/O	-	-
AE13	LPB_AD[2]	Local Peripheral Bus Address/Data Bit 2	I/O	-	-
AD13	LPB_AD[3]	Local Peripheral Bus Address/Data Bit 3	I/O	-	-

Table 17. Comprehensive descriptive pin listing.

Pin	Pin Name	Description	I/O	Alternate	Power Strapping
AG12	LPB_AD[4]	Local Peripheral Bus Address/Data Bit 4	I/O	-	-
AF12	LPB_AD[5]	Local Peripheral Bus Address/Data Bit 5	I/O	-	-
AE12	LPB_AD[6]	Local Peripheral Bus Address/Data Bit 6	I/O	-	-
AD12	LPB_AD[7]	Local Peripheral Bus Address/Data Bit 7	I/O	-	-
AG11	LPB_AD[8]	Local Peripheral Bus Address/Data Bit 8	I/O	-	-
AF11	LPB_AD[9]	Local Peripheral Bus Address/Data Bit 9	I/O	-	-
AD16	DMA_REQ	Local Peripheral Bus: DMA Request	I	-	-
AE16	NC	No Connection	I	-	-
AF15	LPB_INTR	Local Peripheral Bus Interrupt Request	I	-	-
AD17	LPB_PGIO[0]	Local Peripheral Bus Programmable I/O Bit 0	I/O	-	-
AE17	LPB_PGIO[1]	Local Peripheral Bus Programmable I/O Bit 1	I/O	-	-
AF17	LPB_PGIO[2]	Local Peripheral Bus Programmable I/O Bit 2	I/O	-	-
AF16	LPB_PGIO[3]	Local Peripheral Bus Programmable I/O Bit 3	I/O	-	-
AD15	LPB_RD#	Local Peripheral Bus Read Command	O	-	-
AG14	LPB_RESET#	Local Peripheral Bus Reset	O	-	-
AE14	DTACK/RDY#	Local Peripheral Bus Transfer Acknowledge	I	-	-
AE15	LPB_WR#	Local Peripheral Bus Write Command	O	-	-
AC25	IDE_A[0]	IDE Address bit 0	O	DVD host TXD	-
AC26	IDE_A[1]	IDE Address bit 1	O	DVD host HRST	-
AB25	IDE_A[2]	IDE Address bit 2	O	-	-
AD24	IDE_D[0]	IDE Data bit 0	I/O	DVD loader data bit 0	-
AE26	IDE_D[1]	IDE Data bit 1	I/O	DVD loader data bit 1	-
AF25	IDE_D[10]	IDE Data bit 10	I/O	-	-
AE23	IDE_D[11]	IDE Data bit 11	I/O	-	-
AE25	IDE_D[12]	IDE Data bit 12	I/O	-	-
AD23	IDE_D[13]	IDE Data bit 13	I/O	-	-
AE27	IDE_D[14]	IDE Data bit 14	I/O	-	-
AD25	IDE_D[15]	IDE Data bit 15	I/O	-	-
AE24	IDE_D[2]	IDE Data bit 2	I/O	DVD loader data bit 2	-
AF27	IDE_D[3]	IDE Data bit 3	I/O	DVD loader data bit 3	-
AD22	IDE_D[4]	IDE Data bit 4	I/O	DVD loader data bit 4	-
AG26	IDE_D[5]	IDE Data bit 5	I/O	DVD loader data bit 5	-
AF24	IDE_D[6]	IDE Data bit 6	I/O	DVD loader data bit 6	-
AG24	IDE_D[7]	IDE Data bit 7	I/O	DVD loader data bit 7	-
AE22	IDE_D[8]	IDE Data bit 8	I/O	-	-
AG25	IDE_D[9]	IDE Data bit 9	I/O	-	-
AC24	IDE_IOR#	IDE I/O read	O	-	-
AA24	IDE_IOW#	IDE I/O Write	O	DVD loader Data Request	-
A11	VID_HSYNC	Video Output: Horizontal sync	I/O	-	-
AE21	I2CM_SCL	I^2C Master: 2 wire bus interface clock	I/O	-	-
AD21	I2CM_SDA	I^2C Master: 2 wire bus interface data	I/O	-	-
AG22	I2CS_SCL	I^2C Slave: 2 wire bus interface clock	I/O	-	-
AF22	I2CS_SDA	I^2C Slave: 2 wire bus interface data	I/O	-	-
AF23	I2S_WS	I^2S Frame	I/O	-	-

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Pin	Pin Name	Description	I/O	Alternate	Power Strapping
AG20	I2S_SCK	I^2S Clock	I/O	-	-
AG23	I2S_SD	I^2S Data	I	-	-
AC27	IDE_IRQ	IDE Interrupt Request	I	DVD loader Data Ack.	-
AD26	IDE_IORDY	IDE I/O channel ready	I	DVD loader Sector Sync	-
J27	SM_A[0]	System Memory Address Bit 0	O	-	-
K26	SM_A[1]	System Memory Address Bit 1	O	-	-
P24	SM_A[10]	System Memory Address Bit 10	O	-	-
G27	SM_A[11]	System Memory Address Bit 11	O	-	-
U26	SM_A[12]	System Memory Address Bit 12	O	-	-
V25	SM_A[13]	System Memory Address Bit 13	O	-	-
V27	SM_A[14]	System Memory Address Bit 14	O	-	-
V24	SM_A[15]	System Memory Address Bit 15	O	-	-
V26	SM_A[16]	System Memory Address Bit 16	O	-	-
W27	SM_A[17]	System Memory Address Bit 17	O	-	-
W25	SM_A[18]	System Memory Address Bit 18	O	-	-
W26	SM_A[19]	System Memory Address Bit 19	O	-	-
K27	SM_A[2]	System Memory Address Bit 2	O	-	-
W24	FLASH_CS[1]#	Flash Chip Select 1	O	Flash Address Bit 20	-
L26	SM_A[3]	System Memory Address Bit 3	O	-	-
P25	SM_A[4]	System Memory Address Bit 4	O	-	-
K25	SM_A[5]	System Memory Address Bit 5	O	-	-
J26	SM_A[6]	System Memory Address Bit 6	O	-	-
J25	SM_A[7]	System Memory Address Bit 7	O	-	-
H27	SM_A[8]	System Memory Address Bit 8	O	-	-
H26	SM_A[9]	System Memory Address Bit 9	O	-	-
B27	SM_D[0]	System Memory Data Bit 0	I/O	-	-
C26	SM_D[1]	System Memory Data Bit 1	I/O	-	-
K24	SM_D[10]	System Memory Data Bit 10	I/O	-	-
E25	SM_D[11]	System Memory Data Bit 11	I/O	-	-
D27	SM_D[12]	System Memory Data Bit 12	I/O	-	-
D26	SM_D[13]	System Memory Data Bit 13	I/O	-	-
C27	SM_D[14]	System Memory Data Bit 14	I/O	-	-
H25	SM_D[15]	System Memory Data Bit 15	I/O	-	-
M26	SM_D[16]	System Memory Data Bit 16	I/O	-	-
M27	SM_D[17]	System Memory Data Bit 17	I/O	-	-
N25	SM_D[18]	System Memory Data Bit 18	I/O	-	-
T24	SM_D[19]	System Memory Data Bit 19	I/O	-	-
D25	SM_D[2]	System Memory Data Bit 2	I/O	-	-
P26	SM_D[20]	System Memory Data Bit 20	I/O	-	-
P27	SM_D[21]	System Memory Data Bit 21	I/O	-	-
R26	SM_D[22]	System Memory Data Bit 22	I/O	-	-
U24	SM_D[23]	System Memory Data Bit 23	I/O	-	-
U27	SM_D[24]	System Memory Data Bit 24	I/O	-	-
T27	SM_D[25]	System Memory Data Bit 25	I/O	-	-
R27	SM_D[26]	System Memory Data Bit 26	I/O	-	-

Table 17. Comprehensive descriptive pin listing.

Pin	Pin Name	Description	I/O	Alternate	Power Strapping
U25	SM_D[27]	System Memory Data Bit 27	I/O	-	-
N27	SM_D[28]	System Memory Data Bit 28	I/O	-	-
N26	SM_D[29]	System Memory Data Bit 29	I/O	-	-
J24	SM_D[3]	System Memory Data Bit 3	I/O	-	-
T26	SM_D[30]	System Memory Data Bit 30	I/O	-	-
R24	SM_D[31]	System Memory Data Bit 31	I/O	-	-
F24	SM_D[4]	System Memory Data Bit 4	I/O	-	-
E26	SM_D[5]	System Memory Data Bit 5	I/O	-	-
E27	SM_D[6]	System Memory Data Bit 6	I/O	-	-
L24	SM_D[7]	System Memory Data Bit 7	I/O	-	-
F25	SM_D[8]	System Memory Data Bit 8	I/O	-	-
G24	SM_D[9]	System Memory Data Bit 9	I/O	-	-
Y25	FLASH_RYBY#	Flash ready / busy	I	-	-
AA26	IDE_NPCBLID	IDE Cable ID	I	DVD host RDY / HIF	-
AG16	RESET#	Chip reset	I	-	-
A16	TRST#	JTAG: Test Reset	I	-	-
C11	VID_D[0]	Video Output: Y[0]	O	Video Output: B[0]	-
D11	VID_D[1]	Video Output: Y[1]	O	Video Output: B[1]	-
C8	VID_D[10]	Video Output: C[2]	O	Video Output: G[2]	-
D8	VID_D[11]	Video Output: C[3]	O	Video Output: G[3]	-
A7	VID_D[12]	Video Output: C[4]	O	Video Output: G[4]	-
B7	VID_D[13]	Video Output: C[5]	O	Video Output: G[5]	-
C7	VID_D[14]	Video Output: C[6]	O	Video Output: G[6]	-
D7	VID_D[15]	Video Output: C[7]	O	Video Output: G[7]	-
B5	VID_D[16]	-	O	Video Output: R[0]	-
A6	VID_D[17]	-	O	Video Output: R[1]	-
B6	VID_D[18]	-	O	Video Output: R[2]	-
C5	VID_D[19]	-	O	Video Output: R[3]	-
A10	VID_D[2]	Video Output: Y[2]	O	Video Output: B[2]	-
C6	VID_D[20]	-	O	Video Output: R[4]	-
D6	VID_D[21]	-	O	Video Output: R[5]	-
D5	VID_D[22]	-	O	Video Output: R[6]	-
A5	VID_D[23]	-	O	Video Output: R[7]	-
B10	VID_D[3]	Video Output: Y[3]	O	Video Output: B[3]	-
C10	VID_D[4]	Video Output: Y[4]	O	Video Output: B[4]	-
D10	VID_D[5]	Video Output: Y[5]	O	Video Output: B[5]	-
A9	VID_D[6]	Video Output: Y[6]	O	Video Output: B[6]	-
C9	VID_D[7]	Video Output: Y[7]	O	Video Output: B[7]	-
D9	VID_D[8]	Video Output: C[0]	O	Video Output: G[0]	-
B8	VID_D[9]	Video Output: C[1]	O	Video Output: G[1]	-
A8	VID_CLKOUT	Video Output: Video (Pixel) clock Out	O	-	-
B21	PIO0[0]	Programmable I/O Port 0 Bit 0	I/O	-	-
C20	PIO0[1]	Programmable I/O Port 0 Bit 1	I/O	-	-
C24	PIO0[10]	Programmable I/O Port 0 Bit 10	I/O	-	-
A26	PIO0[11]	Programmable I/O Port 0 Bit 11	I/O	-	-

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Pin	Pin Name	Description	I/O	Alternate	Power Strapping
A27	PIO0[12]	Programmable I/O Port 0 Bit 12	I/O	-	-
C25	PIO0[13]	Programmable I/O Port 0 Bit 13	I/O	-	-
B25	PIO0[14]	Programmable I/O Port 0 Bit 14	I/O	-	-
B26	PIO0[15]	Programmable I/O Port Bit 15	I/O	-	-
D20	PIO0[2]	Programmable I/O Port 0 Bit 2	I/O	-	-
C21	PIO0[3]	Programmable I/O Port 0 Bit 3	I/O	-	-
D21	PIO0[4]	Programmable I/O Port 0 Bit 4	I/O	-	-
B22	PIO0[5]	Programmable I/O Port 0 Bit 5	I/O	-	-
C22	PIO0[6]	Programmable I/O Port 0 Bit 6	I/O	-	-
B23	PIO0[7]	Programmable I/O Port 0 Bit 7	I/O	-	-
C23	PIO0[8]	Programmable I/O Port 0 Bit 8	I/O	-	-
B24	PIO0[9]	Programmable I/O Port 0 Bit 9	I/O	-	-
C12	PIO1[0]	Programmable I/O Port 1 Bit 0	I/O	SPI Data In Bit 0	-
B12	PIO1[1]	Programmable I/O Port 1 Bit 1	I/O	SPI Data In Bit 1	-
B15	PIO1[10]	Programmable I/O Port 1 Bit 10	I/O	SPI Sync In	-
C15	PIO1[11]	Programmable I/O Port 1 Bit 11	I/O	-	-
D15	PIO1[12]	Programmable I/O Port 1 Bit 12	I/O	-	-
C16	PIO1[13]	Programmable I/O Port 1 Bit 13	I/O	-	-
D16	PIO1[14]	Programmable I/O Port 1 Bit 14	I/O	-	-
B17	PIO1[15]	Programmable I/O Port 1 Bit 15	I/O	-	-
A12	PIO1[2]	Programmable I/O Port 1 Bit 2	I/O	SPI Data In Bit 2	-
D13	PIO1[3]	Programmable I/O Port 1 Bit 3	I/O	SPI Data In Bit 3	-
C13	PIO1[4]	Programmable I/O Port 1 Bit 4	I/O	SPI Data In Bit 4	-
B13	PIO1[5]	Programmable I/O Port 1 Bit 5	I/O	SPI Data In Bit 5	-
D14	PIO1[6]	Programmable I/O Port 1 Bit 6	I/O	SPI Data In Bit 6	-
C14	PIO1[7]	Programmable I/O Port 1 Bit 7	I/O	SPI Data In Bit 7	-
B16	PIO1[8]	Programmable I/O Port 1 Bit 8	I/O	SPI Clock In	-
B14	PIO1[9]	Programmable I/O Port 1 Bit 9	I/O	SPI Valid In	-
A21	PWRDWN#	PowerDown / PLL Enable	I	-	-
P2	MM_A[0]	Mpeg Memory Address Bit 0	O	-	-
N4	MM_A[1]	Mpeg Memory Address Bit 1	O	-	-
P4	MM_A[10]	Mpeg Memory Address Bit 10	O	-	-
R2	MM_A[11]	Mpeg Memory Address Bit 11	O	-	-
M1	MM_A[2]	Mpeg Memory Address Bit 2	O		-
M2	MM_A[3]	Mpeg Memory Address Bit 3	O	-	-
L1	MM_A[4]	Mpeg Memory Address Bit 4	O	-	-
N3	MM_A[5]	Mpeg Memory Address Bit 5	O	-	-
N2	MM_A[6]	Mpeg Memory Address Bit 6	O	-	-
N1	MM_A[7]	Mpeg Memory Address Bit 7	O	-	-
R3	MM_A[8]	Mpeg Memory Address Bit 8	O	-	-
P1	MM_A[9]	Mpeg Memory Address Bit 9	O	-	-
U2	MM_CAS#	Mpeg Memory Column address strobe	O	-	-
V1	MM_CLK	Mpeg Memory Clock 100 MHz	O	-	-
T1	MM_CS#	Mpeg Memory Chip Select	O	-	-
AC1	MM_D[0]	Mpeg Memory Data Bit 0	I/O	-	-

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Pin	Pin Name	Description	I/O	Alternate	Power Strapping
V3	MM_D[1]	Mpeg Memory Data Bit 1	I/O	-	-
AA1	MM_D[10]	Mpeg Memory Data Bit 10	I/O	-	HOSTMEM_DELAY_2
AA2	MM_D[11]	Mpeg Memory Data Bit 11	I/O	-	HOSTMEM_DELAY_3
U4	MM_D[12]	Mpeg Memory Data Bit 12	I/O	-	HOSTMEM_CLK_SEL
AB2	MM_D[13]	Mpeg Memory Data Bit 13	I/O	-	-
AB3	MM_D[14]	Mpeg Memory Data Bit 14	I/O	-	-
AC2	MM_D[15]	Mpeg Memory Data Bit 15	I/O	-	-
AE3	MM_D[16]	Mpeg Memory Data Bit 16	I/O	-	-
Y4	MM_D[17]	Mpeg Memory Data Bit 17	I/O	-	-
AD3	MM_D[18]	Mpeg Memory Data Bit 18	I/O	-	-
AG1	MM_D[19]	Mpeg Memory Data Bit 19	I/O	-	-
AB1	MM_D[2]	Mpeg Memory Data Bit 2	I/O	-	TEST_MODE0_IN
AF1	MM_D[20]	Mpeg Memory Data Bit 20	I/O	-	-
W3	MM_D[21]	Mpeg Memory Data Bit 21	I/O	-	-
AD2	MM_D[22]	Mpeg Memory Data Bit 22	I/O	-	-
AD1	MM_D[23]	Mpeg Memory Data Bit 23	I/O	-	-
V4	MM_D[24]	Mpeg Memory Data Bit 24	I/O	-	-
AE1	MM_D[25]	Mpeg Memory Data Bit 25	I/O	-	-
AC3	MM_D[26]	Mpeg Memory Data Bit 26	I/O	-	-
W4	MM_D[27]	Mpeg Memory Data Bit 27	I/O	-	-
Y3	MM_D[28]	Mpeg Memory Data Bit 28	I/O	-	-
AF2	MM_D[29]	Mpeg Memory Data Bit 29	I/O	-	-
AA3	MM_D[3]	Mpeg Memory Data Bit 3	I/O	-	TEST_MODE1_IN
AG2	MM_D[30]	Mpeg Memory Data Bit 30	I/O	-	-
AF3	MM_D[31]	Mpeg Memory Data Bit 31	I/O	-	-
U3	MM_D[4]	Mpeg Memory Data Bit 4	I/O	-	TEST_MODE2_IN
T3	MM_D[5]	Mpeg Memory Data Bit 5	I/O	-	TEST_MODE3_IN
Y1	MM_D[6]	Mpeg Memory Data Bit 6	I/O	-	-
V2	MM_D[7]	Mpeg Memory Data Bit 7	I/O	-	PLL_BYPASS_IN
W1	MM_D[8]	Mpeg Memory Data Bit 8	I/O	-	HOSTMEM_DELAY_0
Y2	MM_D[9]	Mpeg Memory Data Bit 9	I/O	-	HOSTMEM_DELAY_1
R4	MM_DQM[0]	Mpeg Memory Input/Output mask Bit 0	O	-	-
R1	MM_DQM[1]	Mpeg Memory Input/Output mask Bit1	O	-	-
U1	MM_DQM[2]	Mpeg Memory Input/Output mask Bit 2	O	-	-
P3	MM_DQM[3]	Mpeg Memory Input/Output mask Bit 3	O	-	-
T4	MM_RAS#	Mpeg Memory Row address strobe	O	-	-
T2	MM_WE#	Mpeg Memory Write Enable for SDRAM	O	-	-
G25	SM_RAS#	System Memory SDRAM Row addr. strobe	O	-	-
D18	UART0_RIN	UART0: Ring Indicator	I	-	-

Table 17. Comprehensive descriptive pin listing.

Pin	Pin Name	Description	I/O	Alternate	Power Strapping
AG19	UART1_RIN	UART1: Ring Indicator	I	-	-
C4	RSET	-	I	-	-
D17	UART0_RTS#	UART0: Request to Send	O	-	-
AD19	UART1_RTS#	UART1: Request to Send	O	-	-
AF19	UART1_RXD	UART1: Receive Data	I	-	-
C18	UART0_RXD	UART0: Receive Data	I	-	-
AG17	SCAN_MODE	Scan Mode	I	-	-
E1	AUD_CLKIN	Serial clock input	I	-	-
F1	AUD_SDIN	Serial data input	I	-	-
L27	SM_CLK	System Memory SDRAM Clock 100 MHz	O	-	-
N24	SM_CLKE	System Memory SDRAM Clock Enable	O	-	-
G26	SM_CS#	System Memory SDRAM Chip select	O	-	-
A20	TCK	JTAG: Test Clock Input	I	-	-
A19	TDI	JTAG: Test Data Input	I	-	-
A18	TDO	JTAG: Test Data Output	O	-	-
A17	TMS	JTAG: Test Mode Select	I	-	-
C17	UART0_TXD	UART0: Transmit Data	O	-	-
AF20	UART1_TXD	UART1: Transmit Data	O	-	-
C1	U	Analog Video output U	O	Analog video output B	-
C3	AVSS_U	VSS U	-	-	-
A25	UART_CLKIN	Receive Clock for Uart 0 and 1	I	-	-
D1	V	Analog video output V	O	Analog video output R	-
D3	AVSS_V	VSS V	-	-	-
B9	VID_CLKIN	Video Output: Video clock In	I	-	-
AF7	VIDIN_D[0]	Video Input Data Bit 0	I	-	-
AE7	VIDIN_D[1]	Video Input Data Bit 1	I	-	-
AA4	VIDIN_D[10]	Video Input Data Bit 10	I	-	-
AE4	VIDIN_D[11]	Video Input Data Bit 11	I	-	-
AB4	VIDIN_D[12]	Video Input Data Bit 12	I	-	-
AG3	VIDIN_D[13]	Video Input Data Bit 13	I	-	-
AC4	VIDIN_D[14]	Video Input Data Bit 14	I	-	-
AD4	VIDIN_D[15]	Video Input Data Bit 15	I	-	-
AD7	VIDIN_D[2]	Video Input Data Bit 2	I	-	-
AF6	VIDIN_D[3]	Video Input Data Bit 3	I	-	-
AE6	VIDIN_D[4]	Video Input Data Bit 4	I	-	-
AD6	VIDIN_D[5]	Video Input Data Bit 5	I	-	-
AF5	VIDIN_D[6]	Video Input Data Bit 6	I	-	-
AE5	VIDIN_D[7]	Video Input Data Bit 7	I	-	-
AD5	VIDIN_D[8]	Video Input Data Bit 8	I	-	-
AF4	VIDIN_D[9]	Video Input Data Bit 9	I	-	-
AG5	VIDIN_HSYNC	Video Input Hsync In	I	-	-
AG4	VIDIN_CLK	Video Input Pixel Clock In	I	-	-
AG6	VIDIN_VSYNC	Video Input Vsync In	I	-	-
D4	VREF	-	O	-	-
D12	VID_VSYNC	Video Output: Vertical sync	I/O	-	-

Table 17. Comprehensive descriptive pin listing.

Pin	Pin Name	Description	I/O	Alternate	Power Strapping
B11	VID_DVLD	Video Output: Video active / Video valid	O	-	-
F27	SM_WE#	System Memory SDRAM Write enable	O	Flash Output enable	-
A22	XIN	27 MHz crystal oscillator input	I	-	-
A23	XOUT	27 MHz crystal oscillator output	O	-	-
B1	Y	Analog video output Y	O	Analog video output G	-
B3	AVSS_Y	VSS Y	-	-	-
AA22	VSS_CORE	-	-	-	-
AA6	VSS_CORE	-	-	-	-
AB22	VSS_CORE	-	-	-	-
AB6	VSS_CORE	-	-	-	-
AB7	VSS_CORE	-	-	-	-
AC11	VSS_CORE	-	-	-	-
AC14	VSS_CORE	-	-	-	-
AC17	VSS_CORE	-	-	-	-
AC20	VSS_CORE	-	-	-	-
AC23	VSS_CORE	-	-	-	-
AC5	VSS_CORE	-	-	-	-
AC8	VSS_CORE	-	-	-	-
E11	VSS_CORE	-	-	-	-
E14	VSS_CORE	-	-	-	-
E17	VSS_CORE	-	-	-	-
E20	VSS_CORE	-	-	-	-
E23	VSS_CORE	-	-	-	-
E5	VSS_CORE	-	-	-	-
E8	VSS_CORE	-	-	-	-
F21	VSS_CORE	-	-	-	-
F22	VSS_IO	-	-	-	-
F6	VSS_IO	-	-	-	-
F7	VSS_IO	-	-	-	-
G22	VSS_IO	-	-	-	-
G6	VSS_IO	-	-	-	-
H23	VSS_IO	-	-	-	-
H5	VSS_IO	-	-	-	-
H6	VSS_IO	-	-	-	-
L11	VSS_IO	-	-	-	-
L12	VSS_IO	-	-	-	-
L13	VSS_IO	-	-	-	-
L14	VSS_IO	-	-	-	-
L15	VSS_IO	-	-	-	-
L16	VSS_IO	-	-	-	-
L17	VSS_IO	-	-	-	-
L23	VSS_IO	-	-	-	-
L5	VSS_IO	-	-	-	-
M11	VSS_IO	-	-	-	-
M12	VSS_IO	-	-	-	-

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Table 17. Comprehensive descriptive pin listing.

Pin	Pin Name	Description	I/O	Alternate	Power Strapping
M13	VSS_IO	-	-	-	-
M14	VSS_IO	-	-	-	-
M15	VSS_IO	-	-	-	-
M16	VSS_IO	-	-	-	-
M17	VSS_IO	-	-	-	-
N11	VSS_IO	-	-	-	-
N12	VSS_IO	-	-	-	-
N13	VSS_IO	-	-	-	-
N14	VSS_IO	-	-	-	-
N15	VSS_IO	-	-	-	-
N16	VSS_IO	-	-	-	-
N17	VSS_IO	-	-	-	-
P11	VSS_IO	-	-	-	-
P12	VSS_IO	-	-	-	-
P13	VSS_IO	-	-	-	-
P14	VSS_IO	-	-	-	-
P15	VSS_IO	-	-	-	-
P16	VSS_IO	-	-	-	-
P17	VSS_IO	-	-	-	-
P23	VSS_IO	-	-	-	-
P5	VSS_IO	-	-	-	-
R11	VSS_IO	-	-	-	-
R12	VSS_IO	-	-	-	-
R13	VSS_IO	-	-	-	-
R14	VSS_IO	-	-	-	-
R15	VSS_IO	-	-	-	-
R16	VSS_IO	-	-	-	-
R17	VSS_IO	-	-	-	-
T11	VSS_IO	-	-	-	-
T12	VSS_IO	-	-	-	-
T13	VSS_IO	-	-	-	-
T14	VSS_IO	-	-	-	-
T15	VSS_IO	-	-	-	-
T16	VSS_IO	-	-	-	-
T17	VSS_IO	-	-	-	-
U11	VSS_IO	-	-	-	-
U12	VSS_IO	-	-	-	-
U13	VSS_IO	-	-	-	-
U14	VSS_IO	-	-	-	-
U15	VSS_IO	-	-	-	-
U16	VSS_IO	-	-	-	-
U17	VSS_IO	-	-	-	-
U23	VSS_IO	-	-	-	-
U5	VSS_IO	-	-	-	-
Y23	VSS_IO	-	-	-	-

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Table 17. Comprehensive descriptive pin listing.

Pin	Pin Name	Description	I/O	Alternate	Power Strapping
Y5	VSS_IO	-	-	-	-
AA5	VDD_CORE	-	-	-	-
AB5	VDD_CORE	-	-	-	-
AC10	VDD_CORE	-	-	-	-
AC15	VDD_CORE	-	-	-	-
AC16	VDD_CORE	-	-	-	-
AC21	VDD_CORE	-	-	-	-
AC22	VDD_CORE	-	-	-	-
AC9	VDD_CORE	-	-	-	-
E12	VDD_CORE	-	-	-	-
E13	VDD_CORE	-	-	-	-
E18	VDD_CORE	-	-	-	-
E19	VDD_CORE	-	-	-	-
E6	VDD_CORE	-	-	-	-
E7	VDD_CORE	-	-	-	-
F23	VDD_CORE	-	-	-	-
G23	VDD_CORE	-	-	-	-
J5	VDD_CORE	-	-	-	-
K5	VDD_CORE	-	-	-	-
M23	VDD_CORE	-	-	-	-
N23	VDD_CORE	-	-	-	-
R5	VDD_CORE	-	-	-	-
T5	VDD_CORE	-	-	-	-
V23	VDD_CORE	-	-	-	-
W23	VDD_CORE	-	-	-	-
AA23	VDD_IO	-	-	-	-
AB23	VDD_IO	-	-	-	-
AC12	VDD_IO	-	-	-	-
AC13	VDD_IO	-	-	-	-
AC18	VDD_IO	-	-	-	-
AC19	VDD_IO	-	-	-	-
AC6	VDD_IO	-	-	-	-
AC7	VDD_IO	-	-	-	-
E10	VDD_IO	-	-	-	-
E15	VDD_IO	-	-	-	-
E16	VDD_IO	-	-	-	-
E21	VDD_IO	-	-	-	-
E22	VDD_IO	-	-	-	-
E9	VDD_IO	-	-	-	-
F5	VDD_IO	-	-	-	-
G5	VDD_IO	-	-	-	-
J23	VDD_IO	-	-	-	-
K23	VDD_IO	-	-	-	-
M5	VDD_IO	-	-	-	-
N5	VDD_IO	-	-	-	-

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Table 17. Comprehensive descriptive pin listing.

Pin	Pin Name	Description	I/O	Alternate	Power Strapping
R23	VDD_IO	-	-	-	-
T23	VDD_IO	-	-	-	-
V5	VDD_IO	-	-	-	-
W5	VDD_IO	-	-	-	-
---	VDD_IO	-	-	-	-
---	VDD_IO	-	-	-	-
---	VDD_IO	-	-	-	-
---	VDD_IO	-	-	-	-
---	VDD_IO	-	-	-	-
---	VDD_IO	-	-	-	-
---	VDD_IO	-	-	-	-
---	VDD_IO	-	-	-	-
---	VDD_IO	-	-	-	-
---	VDD_IO	-	-	-	-
---	VDD_IO	-	-	-	-
---	VDD_IO	-	-	-	-
---	VDD_IO	-	-	-	-
---	VDD_IO	-	-	-	-
---	VDD_IO	-	-	-	-
---	VDD_IO	-	-	-	-
---	VDD_IO	-	-	-	-
AE2	NC				
AF14	NC				
AF26	NC				
AG27	NC				
B20	NC				
E2	NC				
E3	NC				
E4	NC				
H24	NC				
L2	NC				
T25	NC				
W2	NC				

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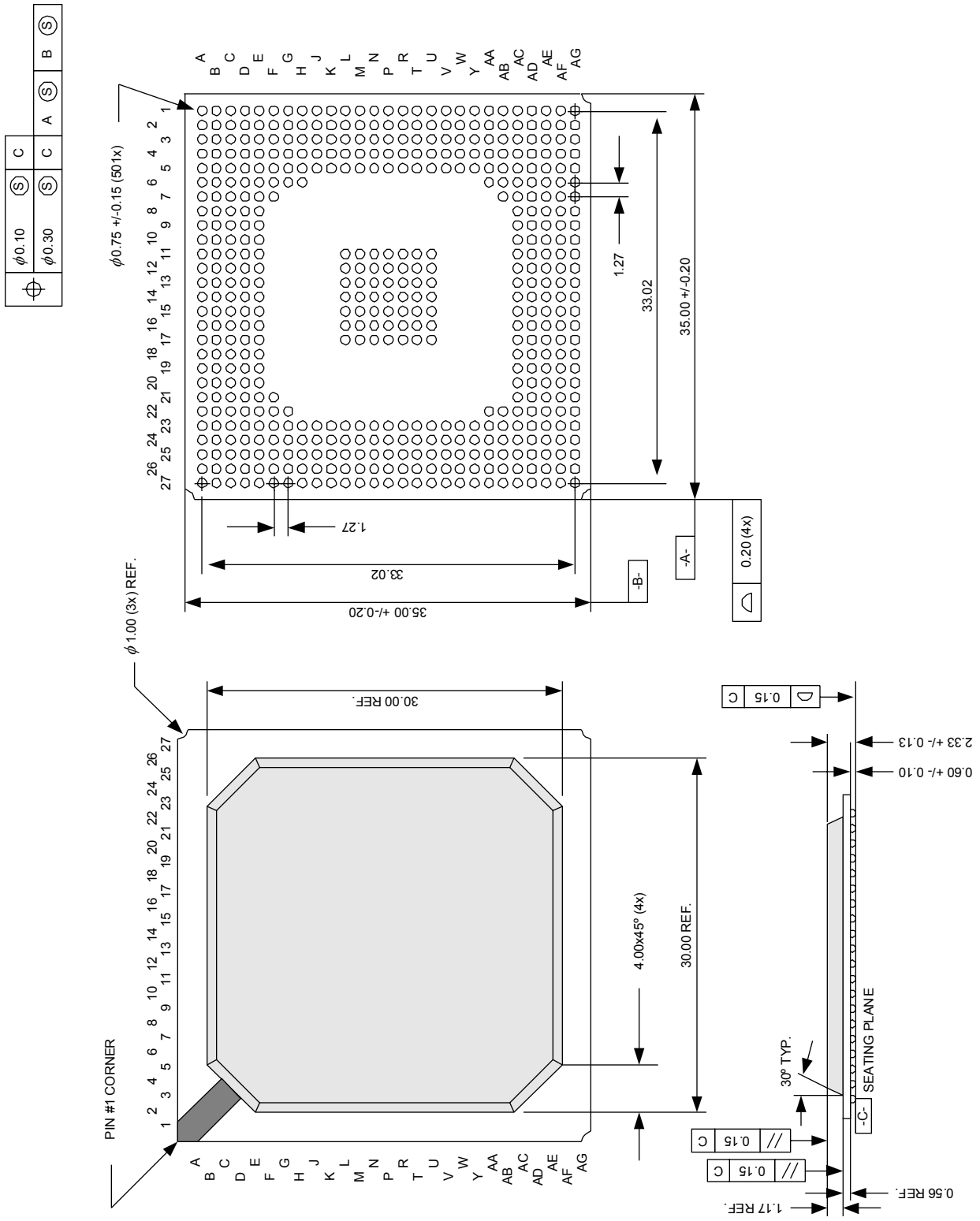
Package Drawing -- 501 BGA



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Datasheet Definitions

Table 18. Datasheet status definitions.

Datasheet Status	Description
Advance	Contains information on a product under development. Features, functionality, and parametric information are target goals, and are subject to change.
Preliminary	Contains information on a product under development that is not fully characterized. The parametric information contains target parameters that are subject to change.
Final	Contains information on a product this is fully characterized and in full production.

Ordering Information

Table 19. Ordering information.

Part Number	Description	Temperature Range	Package
EM8550 EM8550-LF	MPEG-4/DVD Decoder with Macrovision same as above, in lead-free package	0° to 70°C.	501 BGA
EM8551 EM8551-LF	MPEG-4/DVD Decoder without Macrovision same as above, in lead-free package	0° to 70°C.	501 BGA

License requirements

The Dolby Digital feature requires a license from Dolby. The WMA feature requires a license from Microsoft. MPEG video features require license(s) from MPEG-LA. MPEG audio features require license(s) from Via Licensing, Sisvel and/or Thomson.

Sigma Designs Worldwide

Sales Offices			Distributors
USA Headquarters Sigma Designs, Inc. 1221 California Circle Milpitas, CA 95035 +1 (408) 262-9003 +1 (408) 957-9740 FAX www.sigmadesigns.com sales@sdesigns.com	**Europe** Sigma Designs, Inc. 49, Rue des Moissonneurs Brussels, Belgium 1040 +32 496 501234 +32 234 72260 FAX	**Hong Kong** Sigma Designs (Asia) Ltd. Unit 1516, Tower 1, Metroplaza 223 Hing Fong Road Kwai Fong, N.T. Hong Kong +852 2401 7388 +852 2610 2177 FAX	**Japan** Macnica, Inc. Brilliant Technologies Company Macnica Bldg. No 1, 1-6-3 Shin-Yokohama Kohoku-Ku, Yokohama-City, 222-8561 Japan + 81 45 470 9831 + 81 45 470 9832 FAX www.btc.macnica.co.jp
China Sigma Designs China Suite 218, South Block Changsong Building Tairan Industry Zone Shenzhen, PRC 518040 Postcode 518031 +86 755 83435669 +86 755 83435629 FAX	**Japan** Sigma Designs Japan 4-16-8 Nakahara, Mitaka-shi, Tokyo 181-0005, Japan +81 422 79 3067 +81 422 79 3067 FAX	**Taiwan** Sigma Designs Taiwan Far East World Center, C Tower 8F-8, No. 79, Sec. 1 Hsin Tai Wu Road Hsichih, Taipei Hsien Taiwan +886 2 2698 2066 +886 2 2698 2099 FAX	**Korea** Uniquest Korea 8th Floor Dongsung Bldg. 158-24, Samsung-Dong Kangnam-Ku, Seoul 135-090, Korea +82 2 3452 6622 +82 2 3452 6623 FAX www.uniquest.co.kr